Bayer

Technicon RA-XT^{2}System

TECHNICAL SERVICE MANUAL

PUBLICATION NUMBER TF8-7600-10 / 1989

COMPANY CONFIDENTIAL

THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO BAYER CORPORATION AND IS CLASSIFIED COMPANY CONFIDENTIAL. IT IS FURNISHED TO BAYER FIELD SERVICE ENGINEERS FOR MAINTENANCE AND OVERHAUL OF THE SUBJECT EQUIPMENT ONLY. IT SHALL NOT BE DISCLOSED, DUPLICATED, OR USED IN WHOLE OR IN PART FOR ANY OTHER PURPOSE WITHOUT THE PRIOR WRITTEN PERMISSION OF BAYER CORPORATION, DIAGNOSTICS DIVISION.

TABLE OF CONTENTS

Chapter	Title	Page
1	GENERAL DESCRIPTION	1-i
2	FUNCTIONAL DESCRIPTION	2-i
3	ALIGNMENTS & ADJUSTMENTS	3-i
4	ISE MODULE	4-i
5	PREVENTIVE MAINTENANCE	5-i
6	SCHEMATICS	6-i

CHAPTER ONE
GENERAL DESCRIPTION

WARNING

ONLY QUALIFIED SERVICE PERSONNEL WITH EXPERTISE IN ELECTRONICS, MECHANICS, HYDRAULICS, CHEMISTRY, PNEUMATICS, AND OPTICS SHOULD USE THIS MANUAL TO PERFORM THE SERVICE SPECIFIED HEREIN. LACK OF SUCH EXPERTISE MIGHT RESULT IN PERSONAL INJURY AND/OR DAMAGE TO THE SYSTEM.

TABLE OF CONTENTS

Section	Title	Page
1A	INTRODUCTION	1-1
1B	SYSTEM DESCRIPTION	1-1
1B1	Operational Sequence	1-3
1B2	Sample Probe Operational Sequence	1-6
1B3	Analytical Processing	1-6
1B4	Data Handling	1-6
1C	MODULE DESCRIPTIONS	1-7
1C1	Sample Turntable	1-7
1C2	Reagent Turntable	1-7
1C3	Peripump	1-7
1C4	Air Pump and Air Injector Solenoids	1-8
1C5	Reaction Tray Module	1-8
1C6	Colorimeter Assembly	1-8
1C7	Temperature Controllers One and Two	1-9
1C8	Sample and Reagent PD Pumps	1-9
1C9	Sample and Reagent Transfer Assemblies	1-10
1C10	Disk Drive	1-11
1C11	Controls and Indicators	1-11
1D	ILLUSTRATIONS MAJOR MODULES	1-12

LIST OF ILLUSTRATIONS

Figure	Title	Page
1B-1	Functional Diagram of RA-XT System	1-2
1B-2	Reaction Tray Operational Sequence	1-4
1B-3	Reagent Probe Arm Assembly	1-5
1B-4	Reaction Tray Work Cycle	1-5
1B-5	Sample Probe Arm Assembly	1-6
1C-1	Optical System	1-9
1C-2	Sample Transfer Assembly	1-10
1D-1	Front Detail of Temperature Controller Ass抔	1-13
1D-2	Rear View of Temp. Controller & Alarm Board Ass'y	1-13
1D-3	Front View of Reaction Tray with Sensor Disk Removed	1-14
1D-4	Top View of Reagent & Sample Dispense Ass'y	1-15
1D-5	Rear View of Reagent & Sample Dispense Ass'y	1-16
1D-6	Side View of Reagent Tray Drive Assembly	1-17
1D-7	Side View of Sample Tray Drive Assembly	1-18
1D-8	Bottom View of Sample Tray Drive Assembly	1-18
1D-9	Side View of PD Pump Assembly	1-19
1D-10	Detail of PD Pump Sensor	1-19
1D-11	Front View of Colorimeter Assembly	1-20
1D-12	Rear View of Colorimeter Assembly	1-21
1D-13	Side View of Colorimeter Assembly	1-22

1A INTRODUCTION AND ORGANIZATION OF MANUAL

This manual contains theory of operation and servicing information for the Technicon RA-XT system. The manual is divided into ten chapters as follows:

Chapter One, *System Introduction,* provides a high level system description, and other information necessary for a basic understanding of system operation.

Chapter Two, *Functional Descriptions,* contains detailed theory of operation for all system hardware. Several functions may be grouped under one general heading to emphasize the interrelationships amongst individual components.

Chapter Three, *Alignments and Adjustments,* contains the procedures necessary for aligning or adjusting mechanical and electrical assemblies.

Chapter Four, *Troubleshooting,* describes start-up diagnostics and fault messages. Procedures for troubleshooting system hardware also are included.

Chapter Five, *Schematics,* contains electronic and electrical schematic diagrams for all printed circuit boards and electrical systems, with the exception of OEM components. Schematics for OEM components can be found in their respective vendor manuals.

Chapter Six, *Installation,* provides uncrating and assembly instructions for the main system, the ISE module, and the Data Manager.

Chapter Seven, *Preventive Maintenance,* lists components requiring periodic cleaning, oiling, or replacement. PM procedures are provided where necessary.

Chapter Eight, *ISE Module,* provides theory of operation, troubleshooting information, and schematics pertinent to the ISE option.

Chapter Nine, *IDee System,* provides information pertinent to the IDee reader option.

Chapter Ten, *Vendor Manuals,* contains OEM manuals for the Fujitsu thermal printer, Shugart disk drive, and Fluke 1780A touch display module. Information concerning the Convergent Technologies NGEN Data Manager is contained in a separate manual.

1B SYSTEM DESCRIPTION (Refer to Figure 1B-1.)

The Technicon RA-XT system is a bench top, computer-controlled, random access serum or urine chemistry analyzer. The system can perform up to 240 individual assays per hour or 120 assays per hour for those methods that require a blank. The approximate throughput time for an individual assay is between one and ten minutes, depending upon the Technicon method selected. Tests performed on the system require the application of one of four types of analysis to reduce the absorbance data to a reportable concentration value. They are: end point, zero-order rate, first-order rate, and quadratic rate analyses. End point and rate analyses are described in Section I of the *Reference Manual.*

Before sampling can begin, the order in which reagents are positioned on the 24-cup reagent tray must be specified. A maximum of 26 chemistries can be assigned to a reagent tray configuration. Up to 10 reagent tray configurations can be stored on the disk for future use.

A work list is developed by the operator before any samples are processed. The work list designates the method that will be performed for each sample contained in the 30-position sample tray. For each sample specified on the work list, the operator can request any combination of twelve methods listed in the reagent tray configuration. Chemistry methods are described in the *Reference Manual.*

When the system is powered on, it will enter the STANDBY state. In STANDBY, power is applied to the colorimeter lamp, the reagent preheater, the reaction tray air bath, and the system electronics. A 30-minute timer is started to ensure that the temperature of the reagent preheater and reaction tray air bath is stabilized at the desired 30癈 or 37癈. The reagent tray and work list may be entered into the system at this time. Thirty minutes after power on, the system will enter the READY state provided the preheater and air bath temperatures are acceptable.

Figure 1B-1 FUNCTIONAL DIAGRAM OF RA-XT SYSTEM

Sample processing is initiated in the OPERATE mode by entering the number of the work list. In the OPERATE mode the system担 functions are grouped as follows: sample and reagent delivery, analytical processing, and data handling and output. A temperature or hardware problem causes the system to return to the READY mode.

The analytical processing cycle is 15 seconds long, including the time for sample and reagent delivery. The cycle is repeatable for all samples as specified in the work list.

Figure 1B-1 is an overall functional diagram of the system. Sample cups are placed in the sample tray, which is rotated by an a-c motor. Reagents are placed in "boats" in the reagent tray, which also is rotated by an a-c motor.

Sample and reagents are deposited in cuvettes in the reaction tray. D-c motors control the lift and swing of both probes.

Two critical functions of the system are reaction tray rotation and sample and reagent aspiration. These functions are controlled by stepper motors. Stepper motors allow precise control of the amount of rotation, speed of rotation, and damping. The filter wheel also is controlled by a stepper motor because of its requirement for high-speed and precise motion.

The six vertically aligned boxes on the right-hand side of Figure 1B-1 represent the six boards in the card cage. The CPU/Memory/Disk Controller Board is a single-board computer. The RAM Disk Board contains the system RAM, and controls reagent tray rotation and touch display communication. The Serial I/O Board provides LIS, IDEE, and ISE interfaces. The AC Motor Control Board controls sample tray rotation, sample probe lift and swing, and peripump motion. The Stepper Motor Control Board contains five microcomputers that control the stepper motors and printer. The Data Acquisition Board converts colorimeter analog outputs to digital form for processing.

1B1 Operational Sequence (Refer to Figure 1B-2.)

The sample and reagent trays are rotated to bring the sample and reagent cups to their respective aspirate stations. If more than one test is to be performed for a sample, the sample tray will not rotate until all tests have been completed.

The reagent probe is raised from the oil reservoir by the reagent transfer mechanism's vertical motor, and is stopped at the highest point of travel. (This occurs only in the first cycle. After this cycle the probe swings from the reagent cup to the reaction tray cuvette, returning to the oil reservoir only when all the reagents required for each method in the work list have been aspirated; or, when a cuvette of poor quality is the next one to receive reagent. The quality of the cuvettes is determined by a Q.C. scan check.) The reagent positive displacement (PD) pump plunger is driven downward a short distance by the stepper motor, forming an air bubble at the tip of the probe. The probe arm is then positioned over the reagent cup by the transfer mechanism's horizontal motor.

The reagent probe is lowered into the reagent cup by the reagent transfer mechanism's vertical motor. The reagent PD pump energizes and aspirates a precise amount of reagent, which is segmented by air bubbles. Air bubbles are injected into the reagent stream by the action of two pinch valves. The air segmentation maintains a uniform film of random access fluid on the inner wall of the probe.

After aspiration, the probe arm is driven up from the reagent cup to its highest point of travel. The PD pump plunger is again driven downward, which draws the segmented reagent stream into the reagent preheater. The PD pump plunger is then alternately driven up and down by the stepper motor. This pumping action moves the reagent back and forth through the preheater for better heat transfer (see Figure 1B-3).

Figure 1B-2 REACTION TRAY OPERATIONAL SEQUENCE

DESCRIPTION OF CHART

The reaction tray operational sequence chart is divided into three sections: A, B, and C. The operations occurring in each section must be read from top to bottom.

NOTE 1

The time periods between 0 and 15 seconds are approximate, and are shown for descriptive purposes only.

NOTE 2

If more than one test is to be performed on a sample, the sample tray will not rotate until all tests for that sample have been completed.

NOTE 3

The sample delivery sequence for the first assay is initiated approximately 45 seconds after reagent is dispensed into the first reaction cuvette.

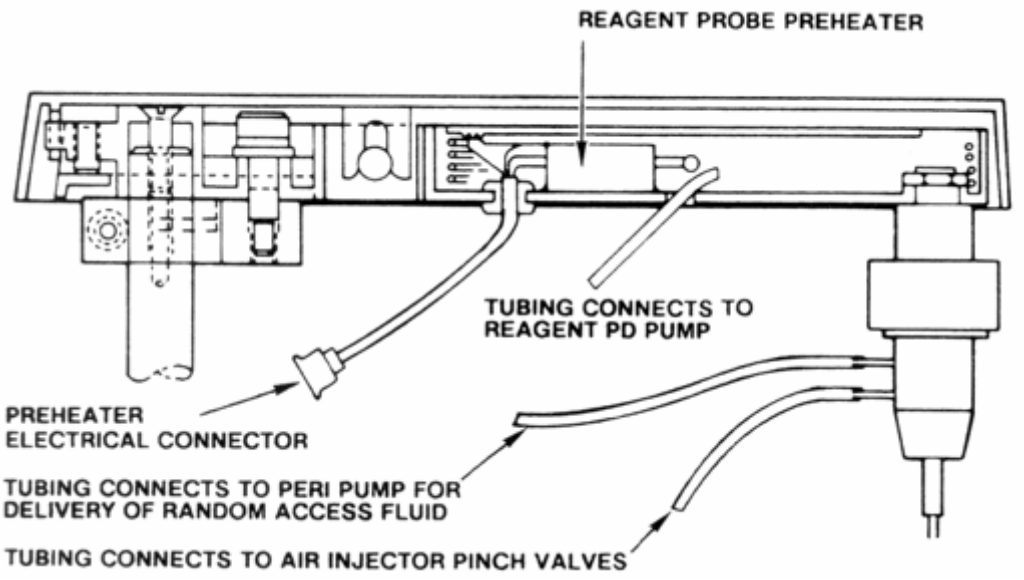


Figure 1B-3 REAGENT PROBE ARM ASSEMBLY

The reagent probe is positioned over the reaction tray by the reagent transfer mechanism's horizontal motor, and lowered into the reaction cuvette by its vertical motor. The pump plunger is driven upward, dispensing the reagent into the cuvette as air bubbles are again injected into the reagent stream. At the same time as reagent is dispensed, the peripump energizes and dispenses a small drop of random access fluid onto the outside of the probe. This removes any reagent carryover. The drop of fluid settles to the bottom of the reaction cuvette. The reagent probe arm is driven up and over to the reagent tray to wait for another cycle.

The sample delivery sequence for the first assay begins approximately 45 seconds after reagent is dispensed into the first reaction cuvette. During this delay, cuvette number one, with reagent, is positioned under the sample dispense station, and cuvette number four under the reagent dispense station. Sufficient time is provided by the delay to obtain reagent blank readings for the first reagent (see Figure 1B-4).

Figure 1B-4 REACTION TRAY WORK CYCLE

1B2 Sample Probe Operational Sequence (Refer to Figure 1B-5.)

The sample probe is raised from the oil reservoir by the sample transfer mechanism's vertical motor. The sample PD pump plunger is driven down by the stepper motor, forming an air bubble at the tip of the probe. The probe arm is positioned over the sample tray by the sample transfer mechanism's horizontal motor, and lowered into the sample cup by the vertical motor. The sample pump plunger is then driven down by the stepper motor as a precise amount of sample is aspirated.

The sample probe is raised from the sample cup and positioned over the reaction tray cuvette. The probe is lowered into the cuvette while the PD pump plunger is driven up to dispense sample into the cuvette. Simultaneously, the peripump is energized, and a drop of random access fluid is pumped onto the outside of the probe to remove any sample carryover. The probe arm is driven up and over to the sample tray to wait for the next cycle.

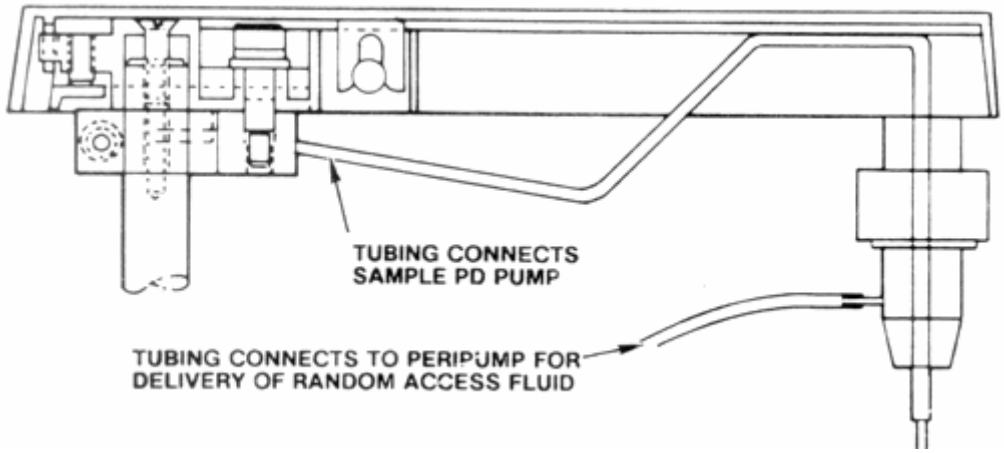


Figure 1B-5 SAMPLE PROBE ARM ASSEMBLY

1B3 Analytical Processing

The reaction tray contains 100 cuvettes. Reagent and sample solutions are mixed and incubated in the cuvettes, and the resulting absorbance is measured. The reaction tray cycle consists of the following routines:

1. Receive sample and/or reagent.
2. Index reaction tray drive abruptly to mix cuvette contents.
3. Read each of 43 cuvettes as they are indexed past the colorimeter.
4. Place the next cuvette at the reagent and sample dispense stations.

When all the samples specified in the work list have been dispensed into the reaction tray cuvettes, the reagent and sample probes are returned to their respective oil reservoirs. The reaction tray continues to cycle in 15-second periods until the processing time required for each assay is completed.

1B4 Data Handling

During the read period, a cuvette is stationed in front of the colorimeter, and the appropriate filter is positioned in the optical path so that the absorbance of the cuvette contents can be read.

The analog sample and reference signals from the preamplifier boards are routed to the analog-to-digital converter board. The sample and reference signals are multiplexed on the A/D board and converted to a frequency equivalent of the analog voltage. The voltage-to-frequency converter provides an accurate conversion of analog signals into a train of constant width and amplitude pulses at a rate directly proportional to the analog signal amplitude.

The pulse train is sent to the data acquisition board where it is loaded into a counter. The counter retains the data until needed by the system microprocessor (磼).

The sample data input to the system 磼 is used in the respective algorithms for first-order rate, zero-order rate, quadratic rate, and end point methods. The computed results are then output to the printer. If desired, the data may be output to the TTY/RS-232 port located on the serial I/O board.

1C MODULE DESCRIPTIONS

The following section provides brief functional and hardware descriptions of modules used in the RA-XT system. The photographs at the end of this Chapter identify the hardware components and assemblies.

1C1 Sample Turntable (Refer to IPB Figure 6.)

Sample cups are moved sequentially to the aspirate position by the counterclockwise rotation of the sample tray. The sample tray can hold up to thirty 2-mL sample cups. The turntable, which supports the sample tray, is directly coupled to the drive shaft of a 115-V a-c, 1-RPM motor. An encoder disk with thirty equally spaced strobe holes around the outer edge is attached to the motor drive shaft.

A tray position sensor sends a signal back to the AC Motor Control Board to stop tray rotation when a strobe hole is positioned under the sensor.

The sample turntable is a self-contained module that includes the a-c motor, sensor control board, and turntable assembly.

1C2 Reagent Turntable (Refer to IPB Figure 6.)

Reagent cups are moved to the aspirate position as chemistry requirements dictate. The reagent tray can hold up to 24 boats containing 22 reagents and two reagent blanks. The reagent turntable, which supports the reagent tray, is coupled directly to the drive shaft of a 115-V a-c, 20-RPM motor. An encoder disk mounted on the motor drive shaft detects when a reagent has arrived at the aspirate station.

The reagent turntable, like the sample turntable, is a self-contained module that includes the a-c motor, sensor control board, sensor board assembly, and turntable assembly.

1C3 Peripump

Random access fluid is pumped to the sample and reagent probes by the peripump. The fluid is pumped from the reservoir bottle, through the pump tubing, to the tip of the probes during a prime cycle. The random access fluid maintains sample integrity by preventing the sample from coming into contact with the inner wall of the probe. When sample or reagent is dispensed into the reaction cuvette, the peripump is energized, and fluid is pumped onto the outside of the probe to clean it.

The pump consists of a platen and a rotor with four rollers, which is driven by an a-c synchronous motor. The 115-V a-c motor rotates clockwise at 20 RPM for 60-Hz systems, or 17 RPM for 50-Hz systems. The platen is spring loaded and exerts a force of 6.5 pounds against the rollers.

An encoder disk, with four slots positioned 90 degrees apart, is attached to the rotor. The four slots provide rotor position information to the system 磼. When the pump stops, one of the four rollers should be at the center of the platen. The pump sensor can be adjusted to meet this condition.

The peripump assembly includes the a-c motor, the platen and motor assembly, and the sensor control board.

1C4 Air Pump and Air Injector Solenoids

The air pump is driven by a synchronous a-c motor to produce 5 PSI of pressurized air. The 120-RPM motor is supplied 115 V ac when system power is turned on, and is coupled to the piston shaft by an eccentric. The piston delivers the pressurized air to a dual check valve. The check valve allows atmospheric air to be drawn in on the piston's downstroke, and compressed air to be released to the air injector pinch valves on the upstroke.

Air pressure can be adjusted to 5 PSI by loosening the motor hold down screws, and sliding the motor up or down.

The air injector pinch valves are program controlled to inject air bubbles into the reagent stream when the probe is aspirating reagent, and again when dispensing reagent into the reaction cuvettes. The pinch valves require 24 V d-c to operate. They are controlled by logic level signals from the AC Motor Control Board located in the card cage. Logic level commands are converted to power level drive signals on the air injector control board.

1C5 Reaction Tray Module (Refer to IPB Figure 8.)

The reaction tray module contains the drive mechanism for the 100-position cuvette tray. It also circulates warm air around the tray, which is required for the chemical reactions in the cuvettes.

The reaction tray module drive plate is belt driven by a stepper motor. Belt tension is maintained by a spring attached to the stepper motor mounting plate. The cyclic mix, slew, and read periods of the tray are program controlled by an 8741A CPU on the Stepper Motor Controller Board located in the card cage. Home and cuvette positions 25, 50, 75, and 1 are monitored by home and 90 degree sensors. These sensors detect cutouts positioned every 90 degrees on the sensor disk. The stepper motor sensor board, which is mounted externally to the reaction module enclosure, converts the logic level commands to power level drive signals required by the motor. The board also transfers the home and 90 degree sensor signals to the CPU.

Heat in the module is generated by a wire-wound heater. Should the temperature exceed 60 degrees centigrade, a thermostat in series with the heating element opens and interrupts one side of the power line. A venturi fan, located above the heater assembly, circulates the warm air within the enclosure. A thermistor close to the cuvette area provides feedback signals to a temperature controller, which maintains the temperature at a constant 30 or 37 degrees centigrade. An opening is provided on the side of the enclosure for the colorimeter assembly. An interlock switch on the upper edge of the enclosure alerts the system 礙 that the cover has been removed from the reaction tray and warm air is escaping. When the reaction tray cover is off, the system will not operate.

1C6 Colorimeter Assembly (Refer to Figure 1C-1.)

The Colorimeter Assembly is mounted on the side of the reaction tray enclosure. It measures the changes in optical absorbance associated with rate, fixed point, and end point chemistries. The colorimeter is a self-contained unit consisting of the stepper motor, light source, filter wheel, and stepper motor sensor board.

A stepper motor driven filter wheel enables the optical system to make absorbance measurements at any one of six discrete wavelengths. The interference filters are selected to match the center wavelengths of the system chemistries, and span the spectral range from 340 nm to 600 nm. The output of the tungsten halogen light source is held constant by a 7.2-V d-c regulated power supply when the system is in the operate mode.

As shown in Figure 1C-1, light rays from the source lamp are collimated by condenser lens L1, and directed through interference filter F1. Light from the filter is collected by projection lens L2 to form a unity image of the lamp in the sample cuvette. Light from the cuvette is collected by condenser lenses L3 and L4, and imaged onto the photodetector surface. Apertures A1 and A2 pass the light rays that form the image of the filament on the cuvette. All other rays are blocked from the optical system. A thin quartz beamsplitter, placed at a 45-degree angle to the main sample beam, reflects about eight percent of the total light output to the reference photodetector. Lens L5 collects light from the beamsplitter and images it onto the reference photodetector.

Figure 1C-1 OPTICAL SYSTEM

The warm air circulated in the reaction tray chamber also flows over the colorimeter assembly to provide a stable 30癈 or 37癈 environment. A stable temperature surrounding the optical system is required for the colorimeter to produce accurate results.

The filter wheel is belt driven by the stepper motor and is program controlled by an 8741A CPU on the Stepper Motor Controller Board.

The home position of the filter wheel is detected by a sensor that monitors a cutout in the edge of the filter wheel. The-stepper motor sensor board, located on the colorimeter assembly, converts logic level control signals to power level drive signals for the stepper motor. It also transfers the home sensor signal to the 8741A CPU.

1C7 Temperature Controllers One and Two

The Technicon RA-XT system contains two temperature controllers. Controller 1 maintains the temperature of the air circulating in the reaction module enclosure at 30癈 or 37癈, and controls the temperature in the Reaction Tray Preheater. Controller 2 maintains the temperature of the reagent probe preheater at a preset level, so that the reagent can be heated to the assay temperature of either 30癈 or 37癈. If the temperatures go above or below preset limits, an alarm circuit alerts the system 礹. The controller boards are mounted on the Temperature Controller. Assembly plate, which includes the Alarm Control Board.

1C8 Sample and Reagent Positive Displacement Pumps

The purpose of the sample and reagent positive displacement pumps is to aspirate and dispense precise quantities of liquid as directed by the main system program. The pump assemblies consist of a syringe, stepper motor, stepper sensor control board, home sensor, and rack and pinion drive assemblies.

The two pumps are identical except for the volume of the syringe used in each pump. The reagent syringe volume is 500 礒, while the sample syringe volume is 50 礒. The sample pump delivers between 1 礒 and 30 礒 of sample. Each pump is driven by a stepper motor coupled to a rack and pinion assembly. The precise distance travelled by the plunger stroke is controlled by an 8741A CPU on the Stepper Motor Controller Board. A stepper motor sensor board in each pump assembly converts the logic level control signals to power level drive signals. The board also transfers the home sensor signals to the 8741A CPU.

1C9 Sample and Reagent Transfer Assemblies (Refer to Figure 1C-2.)

The sample and reagent transfer mechanisms impart vertical and horizontal (swing) motion to the reagent and sample probe arms in order to transport sample and reagents from the turntables to the reaction tray.

The vertical motion is achieved by a yoke assembly driven by a 24-V d-c motor for accurate stopping characteristics. One half revolution of the motor will drive the probe shaft up to a point where the shaft guide pin clears the groove in the guide block. At the upper limit, a cutout in the sensor disk turns on a sensor that signals the AC Motor Control Board to stop the motor.

In the up position the probe arm can be rotated to any one of the three horizontal positions: oil, aspirate, and dispense. The swing motion of the probe is achieved by the linkage between a second 24-V d-c drive motor and the probe shaft. Motor rotation is counterclockwise for the sample transfer mechanism; and clockwise for the reagent transfer mechanism.

Figure 1C-2 SAMPLE TRANSFER ASSEMBLY

Technicon RA-XT systems equipped with the ISE option contain a sample transfer mechanism that differs by the addition of a second horizontal swing motor for the ISE resample probe.

An encoder disk coupled to the drive motor shaft, and sensors at the oil, aspirate, and dispense positions informs the CPU when the motor is over the requested position. The AC Motor Control Board then shuts off power to the motor. The probe shaft guide pin at this time will be positioned over the proper groove in the guide block.

The probe arm remains over the requested position until the system CPU commands the vertical motor to drive the yoke and probe shaft assembly down. In the down position, the cutout in the sensor disk turns on a sensor. The sensor signal informs the CPU of the probe position, and the AC Motor Control Board stops the motor. The vertical motor always drives in one-half cycles in a CW direction.

The transfer assemblies consist of two 24-V d-c motors, an encoder disk coupled to each motor drive shaft, two sensors for vertical position information, and three sensors for horizontal position information. Two identical DC Sensor Control Boards convert the logic level commands from the system CPU to power level signals for the respective motors. The boards also transfer the sensor signals to the CPU.

1C10 Disk Drive

The RA-XT employs a mini floppy disk drive to download the system operating program to the 512K dynamic RAM memory resident on the RAM Disk Board. The drive uses a 51/4-inch double-sided, double-density disk.

The drive unit is driven by a d-c motor, and requires +5 V d-c and +12 V d-c supply voltages from the host system to operate. The disk controller, part of the main system CPU board, provides the control commands to the drive unit to read data from and to write data onto the disk. Chemistry parameters, profiles, system configuration parameters, and up to 10 reagent tray configurations can be stored on the disk.

1C11 Controls and Indicators

- **Infotouch Display**

Operator control of the Technicon RA-XT system is implemented through the Fluke 1780A Infotouch Display Module. This module contains a touch sensitive screen overlay that replaces conventional keyboards for data entry and system control functions. Error messages also are displayed on this module.

- **Printer Assembly**

The printer assembly consists of a 40-column thermal printer and a controller board. Data is output to the printer by the Stepper Motor Controller Board. Voltage requirements for the printer assembly are +5 V d-c and +24 V d-c.

- **Indicator Panel**

The Indicator Panel contains the clock module, and system status and alarm lamps. The clock module can be configured for 50/60-Hz and 12-hour/24-hour (military) display operation. System status lamps - STANDBY, READY, OPERATE - are controlled by the RAM Disk board. The two heater alarm lamps (reaction and reagent) are controlled by the Temperature Controller board. Finally, the Reaction Tray Preheater lamp is illuminated by a relay when the reaction tray preheater is on.

1D ILLUSTRATIONS AND LOCATIONS OF MAJOR MODULES

This Section contains photographs of some key Technicon RA-XT system components and modules. For more detailed information, refer to the system *Illustrated Parts Breakdown.*

Following is a list of the photographs included in this Section:

1D-1 Front Detail of Temperature Controller Assembly

1D-2 Rear View of Temperature Controller and Alarm Board Assembly

1D-3 Front View of Reaction Tray with Sensor Disk Removed

1D-4 Top View of Reagent and Sample Dispense Assembly

1D-5 Rear View of Reagent and Sample Dispense Assembly

1D-6 Side View of Reagent Tray Assembly

1D-7 Side View of Sample Tray Assembly

1D-8 Bottom View of Sample Tray Assembly

1D-9 Side View of Positive Displacement Pump Assembly

1D-10 Detail of Positive Displacement Pump Sensor

1D-11 Front View of Colorimeter Assembly

1D-12 Rear View of Colorimeter Assembly

1D-13 Side View of Colorimeter Assembly

Figure 1D-1 FRONT DETAIL OF TEMPERATURE CONTROLLER ASSEMBLY

Figure 1D-2 REAR VIEW OF TEMPERATURE CONTROLLER AND ALARM BOARD ASSEMBLY

Figure 1D-3 FRONT VIEW OF REACTION TRAY WITH SENSOR DISK REMOVED

Figure 1D-4 TOP VIEW OF REAGENT AND SAMPLE DISPENSE ASSEMBLY

Figure 1D-5 REAR VIEW OF REAGENT AND SAMPLE DISPENSE ASSEMBLY

Figure 1D-6 SIDE VIEW OF REAGENT TRAY DRIVE ASSEMBLY

Figure 1D-7 SIDE VIEW OF SAMPLE TRAY DRIVE ASSEMBLY

Figure 1D-8 BOTTOM VIEW OF SAMPLE TRAY DRIVE ASSEMBLY

Figure 1D-9 SIDE VIEW OF POSITIVE DISPLACEMENT PUMP ASSEMBLY

Figure 1D-10 DETAIL OF POSITIVE DISPLACEMENT PUMP SENSOR

Figure 1D-11 FRONT VIEW OF COLORIMETER ASSEMBLY

Figure 1D-12 REAR VIEW OF COLORIMETER ASSEMBLY

Figure 1D-13 SIDE VIEW OF COLORIMETER ASSEMBLY

CHAPTER TWO
FUNCTIONAL DESCRIPTIONS

WARNING

ONLY QUALIFIED SERVICE PERSONNEL WITH EXPERTISE IN ELECTRONICS. MECHANICS, HYDRAULICS, CHEMISTRY, PNEUMATICS, AND OPTICS SHOULD USE THIS MANUAL TO PERFORM THE SERVICE SPECIFIED HEREIN. LACK OF SUCH EXPERTISE MIGHT RESULT IN PERSONAL INJURY AND/OR DAMAGE TO THE SYSTEM.

TABLE OF CONTENTS

Section	Title	Page
2A	INTRODUCTION	2-1
2B	A-C & D-C MOTOR FUNCTIONS	2-1
2B1	Functional Description of Motor Control Circuits	2-1
2B2	AC Motor Control Board Description	2-4
2B3	Data Transfer Between 礙 & AC Motor Ctl. Bd.	2-4
2B4	Sample Tray Motor On Command	2-5
2B5	Sample Probe Lift Motor Command	2-5
2B6	Sample Probe Swing Motor Command	2-6
2B7	Reagent Probe Motor On Commands	2-6
2B8	Reagent Tray Motor Control	2-6
2B9	X Reset	2-9
2B10	Peripump Motor Control	2-9
2B11	Air Injection Timing Description	2-9
2B11.1	Circuit Description	2-9
2B12	AC Motor & Sensor Control Bd. Description	2-10
2B13	DC Motor Sensor Control Bd. Description	2-10
2B14	Air Injection Control Bd. Description	2-11
2C	STEPPER MOTOR FUNCTIONS	2-17
2C1	Stepper Motor Description	2-17
2C1.1	Basic Stepper Motor Operation	2-17
2C1.2	Basic Stepper Motor Characteristics	2-20
2C1.3	Stepper Motor Supply Voltage	2-20
2C2	Stepper Motor Homing	2-21
2C2.1	Reaction Tray Home	2-21
2C2.2	Filter Wheel Home	2-21
2C2.3	PD Pump Home	2-21
2C3	Stepper Motor Driven Devices	2-22
2C3.1	Reaction Tray	2-22
2C3.2	Filter Wheel	2-23
2C3.3	PD Pumps	2-23
2C4	Stepper Motor Control Circuits	2-24
2C4.1	Sensor Assemblies	2-24
2C5	Stepper Motor Functional Diagram	2-24

2C6	Stepper Motor Controller Bd. Description	2-25
2C6.1	Program Selection of 8741A CPU	2-25
2C6.2	Data Transfer Between 礙 & Stepper Ctlr. Bd.	2-25
2C6.3	Stepper Motor Commands: Reaction Tray & PD Pumps	2-26
2C6.4	Stepper Motor Commands for Filter Wheel	2-26
2C7	Heat Sink Assembly	2-27
2C7.1	Circuit Description	2-27
2C8	Stepper Motor/Sensor Board	2-27
2C8.1	Circuit Description	2-27
2C8.2	Reaction Tray Stepper Motor Half-step Operation	2-28
2C8.3	Filter Wheel & PD Pump Full-step Operation	2-29

TABLE OF CONTENTS (continued)

Section	Title	Page
2D	COLORIMETER	2-33
2D1	A/D Converter Board Description	2-34
2D2	Data Acquisition Board Description	2-34
2D2.1	Selection of PIA U9 or U10 by 礙	2-35
2D2.2	Circuit Description	2-35
2D2.3	Sample and Reference Read Time Commands	2-36
2D3	Source Lamp Power Supply	2-36
2E	FRONT PANEL ASSEMBLIES	2-41
2E1	Touch Display Module	2-41
2E1.1	Touch Display Communication	2-41
2E1.1.1	Start-up Diagnostics	2-41
2E1.1.2	Touch Screen Inputs	2-43
2E1.1.3	Display Control	2-43
2E1.1.4	Character Generation	2-43
2E2	Indicator Panel	2-44
2E2.1	Clock Module	2-44
2E2.1.1	Programmable Inputs	2-44
2E2.2	Indicator Panel Lamps	2-46
2E2.3	Operating Mode Lamps	2-47
2E3	ALARM RESET and PAPER FEED Switches	2-47
2E4	Printer	2-49
2E4.1	Printer Interface	2-51
2E5	Reaction Tray Preheater	2-52
2E5.1	Temperature Control	2-52
2E6	Fluorescent Lamp	2-53
2E6.1	Circuit Operation	2-53
2F	TEMPERATURE CONTROLLERS 1 & 2	2-54
2F1	Reaction Module Heater Control Circuit	2-54
2F2	Reagent Preheater Control Circuit	2-54
2F3	Reaction Module Heater & Reagent Preheater	2-58
2F4	Controller Boards One and Two Circuits	2-58
2F5	Alarm Control Board	2-58
2G	CPU/MEMORY/DISK CONTROLLER BOARD	2-59
2G1	RAM Disk Board Memory	2-60
2G2	DMA Control	2-61
2G3	Ready Controller	2-62
2G4	Bus Controller	2-63
2G5	Status Decoder	2-64
2G6	Address Decoder	2-65
2G7	Memory Decoder	2-65
2G8	Serial I/O	2-65

2G9	Disk Controller	2-66
2G9.1	Disk Controller IC	2-66
2G9.2	Decoding/Encoding Circuits for Multiplexed Lines	2-68
2G9.3	Data Separation Circuits	2-68
2G9.4	Double Density Write Circuitry	2-68
2G10	Jumper Settings	2-68
2H	LIS, IDee, & ISE INTERFACE	2-71
2H1	8251A Interface Device	2-71
2H1.1	Asynchronous Transmission	2-74
2H1.2	Asynchronous Reception	2-74
2H2	Programmable Baud Rate Generator	2-75
2H3	Data Transfer to Microprocessor	2-75
2I	A-C & D-C POWER DISTRIBUTION	2-76

LIST OF ILLUSTRATIONS

Figure	Title	Page
2B-1	A-c & D-c Motor Control Circuits	2-2
2B-2	A-c & D-c Motor Control Circuits	2-3
2B-3	Reagent Tray Motor Control	2-8
2BFO1	Sample Tray & Sample Probe Lift & Swing Motor Control Circuits	2-13
2BFO2	Peripump & Pinch Valve Circuits	2-15
2C-1	Stepper Motor Windings	2-17
2C-2	Four Stepper Motor Positions - Full-step Mode	2-18
2C-3	Eight Stepper Motor Positions - Half-step Mode	2-18
2C-4	Stepper Motor	2-19
2C-5	Stepper Motor Full-step Operation	2-20
2C-6	Stepper Motor Half-step Operation	2-20
2C-7	Supply Voltage to Stepper Motor Windings	2-21
2C-8	Reaction Tray 90?From Home	2-22
2C-9	Filter Wheel Rotated to Place Filter 2 in Read Position	2-23
2C-10	Stepper Motor Winding Patterns	2-28
2C-11	Simplified Stepper Motor Circuit	2-28
2CFO1	Filter Wheel Stepper Motor Circuits	2-31
2D-1	Functional Diagram of Colorimeter	2-33
2D-2	Functional Diagram of 7.2-V d-c Power Supply	2-37
2DFO1	Colorimeter Circuits	2-39
2E-1	Touch Display Communication	2-42
2E-2	Character Load & Shift Timing	2-43
2E-3	Indicator Panel	2-45
2E-4	RAM Disk Bd. Indicator Control & Switch Monitoring	2-46
2E-5	Mode Change Logic	2-48
2E-6	Printer Dot Matrix	2-49
2E-7	Thermal Printer Exerciser Test Printout	2-49
2E-8	Thermal Printer Paper Loading	2-50
2E-9	Thermal Printer Self-test Printout	2-50
2E-10	Printer Interface	2-51
2E-11	Reaction Tray Preheater Interconnect Diagram	2-52
2F-1	Temperature Controller Circuits	2-55
2F-2	Reaction Module Enclosure 30癈 Thermistor Sensing Circuit	2-56
2F-3	Reaction Module Enclosure 37癈 Thermistor Sensing Circuit	2-56
2F-4	Reagent Probe Arm Preheater 30癈 Thermocouple Sensing Circuit	2-57
2F-5	Reagent Probe Arm Preheater 37癈 Thermocouple Sensing Circuit	2-57
2G-1	DMA Control	2-61
2G-2	Ready Controller	2-63
2G-3	Bus Decoder	2-63
2G-4	Status Decoder	2-64
2G-5	Address Decoder	2-64
2G-6	Memory Decoder	2-65
2G-7	Serial I/O	2-66

2G-8	Disk Control Circuitry	2-67
2GFO1	CPU/Memory/Disk Controller Block Diagram	2-69
2H-1	LIS, IDee, ISE Interconnect Diagram	2-72
2H-2	Serial I/O Bd.	2-73
2H-3	Status Read Format	2-74
2H-4	RS-232 Transmit & Receive Characters	2-75
2I-1	Power Distribution to RA-XT Modules	2-76

LIST OF TABLES

Table Number	Title	Page
2-1	U13 & U19 Data Flow	2-5
2-2	U21 Data Flow	2-7
2-3	Stepper Motor Revolutions vs. Reaction Tray Rotation	2-22
2-4	Filter Positioning	2-23
2-5	8741A Data Flow	2-26
2-6	Sample/Reference Channel Selection	2-34
2-7	U29 Data Flow	2-41
2-8	CPU Bd. Jumper Settings	2-68
2-9	A-c & D-c Power Distribution	2-77

2A INTRODUCTION TO FUNCTIONAL DESCRIPTIONS

This Chapter provides detailed theory of operation for each system function. Sections 2B and 2C describe several interrelated motor functions. Section 2D describes the, colorimeter, exclusive of the filter wheel function, which is described in Section 2B. Section 2E describes the hardware on the front panel, including the touch display module, indicator panel, reaction tray preheater, printer, and the fluorescent light fixture. Section 2F describes the temperature controller circuitry. Section 2G describes the CPU/Memory/Disk Controller Board and the RAM Disk Board memory. In Section 2H, the Serial I/O Board, which contains the LIS, IDee, and ISE interfaces, is described. Finally power distribution is described in Section 2I.

Section 2B describes motor functions, excluding the stepper motor functions described in Section 2C. These functions - sample tray motion, and sample and reagent probe lift and swing - are interrelated because they are all controlled by the AC Motor Control Board. The optional IDee reader is controlled by this same board, and is described in the "IDee System" section of the manual. Reagent tray motion is controlled by the RAM Disk board, also described in Section 2B.

Section 2C describes the stepper motor functions: reaction tray, filter wheel, and sample and reagent PD pumps. These functions are all controlled by the Stepper Motor Controller Board. Each motor is associated with a motor and sensor control board. The four motor and sensor control boards are almost identical to one another, and are used to transfer sensor signals and to actuate relay switches. A brief discussion of stepper motor theory also is included.

2B A-C AND D-C MOTOR FUNCTIONS (Refer to Figures 2B-1 and 2B-2.)

D-c motors control the vertical and horizontal motion of the reagent and sample probe arms. D-c motors are used for these functions because their braking characteristics are better than the braking characteristics of a-c motors.

A-c motors control rotation of the reagent and sample trays, and movement of the peripump.

The AC Motor Control Board (P/N 108-B199-01) generates the logic command signals for all a-c and d-c motor and sensor control boards, except the one associated with the reagent tray. Logic signals for the reagent tray motor and sensor control board come from the RAM Disk board. The DC Motor & Sensor Control boards, on command, transfer 24 V dc through the board to operate the d-c motors.

The AC Motor & Sensor Control boards, on command, transfer 115 V ac through the board to operate the a-c motors.

2B1 Functional Description of Motor Control Circuits

When the system program dictates, the 磼 board issues a device address code to the AC Motor Control Board. The AC Motor Control Board decodes the address and enables the desired peripheral interface adapter (PIA). The selected PIA then communicates with the main 磼 over the data bus. The AC Motor Control Board has two 8255 PIAs - U13 and U19. Ports A and C on PIA U13 are configured as output ports. U13 input port B receives status signals from the sensors.

Port A of PIA U19 is an output, port B is an input; and port C is used for both input and output.

The logic level output commands from the peripheral devices control a D flip-flop and logic gates, which ultimately produce the MOTOR ON and MOTOR OFF commands. The commands are issued to the AC and DC Motor & Sensor Control boards.

For example, when the AC Motor Control Board outputs a command to turn on the sample tray motor, the following sequence occurs. The command line from the AC Motor Control Board changes to logic 0. The switch on the AC Motor & Sensor Control board closes and allows 115V ac to energize the sample tray motor. The sample tray rotates to the next consecutive sample cup position, and a sensor issues a logic 1 status signal to the AC Motor Control Board. The status signal is inverted to logic 0, terminates the sample tray MOTOR ON command, and provides status to the main 磼 through the B port of the PIA.

Figure 2B-1 A-C AND D-C MOTOR CONTROL CIRCUITS

Figure 2B-2 A-C AND D-C MOTOR CONTROL CIRCUITS

The AC Motor Control Board also.

a) Generates commands to control pinch valve solenoids.

b) Monitors the reaction tray cover interlock switch, and inhibits system operations if the switch is open.

c) Reduces the optics lamp voltage to 5.0 volts when the system is in STANDBY.

d) Generates the -IDEE MTR singal, which turns on the motor in the IDee reader head.

2B2 AC Motor Control Board Description (Refer to Schematic 108-C199.)

The AC Motor Control Board provides the command signals for

a) Vertical motion of sample and reagent probe arms.

b) Horizontal motion of sample and reagent probe arms.

c) Sample and reagent tray rotation.

d) Operation of the peripump.

e) Actuation of pinch valves to enable injection of air bubbles into the reagent stream.

f) Reduction of the colorimeter lamp voltage from 7.2 volts to 5.0 volts when the system is in STANDBY.

g) Informing the system CPU to start the thirty minute timer to ensure that the sensor for the fan and two temperature controllers is stable before allowing system operation.

h) Monitoring the reaction tray cover interlock switch. When the interlock switch is open, system operation is inhibited.

The AC Motor Control Board communicates with the main 礙 board through two 8255 PIAs: U13 (schematic sheet 2) and U19 (schematic sheet 3). The PIA consists of a data bus buffer, read/write control logic, and three ports. The ports are configured into a basic input/output mode (mode 0) by a control word from the main 礙.

Ports A and C on PIA U13 are output ports, and port B is an input port. Port A on PIA U19 is an output port, port B is an input port, and port C is divided into four inputs and four outputs.

PIA U13 outputs commands for the sample probe lift motor, the sample probe swing motor, the sample tray motor, the peripump motor, the air bubble injection solenoids, and the reduction of the colorimeter lamp voltage in STANDBY.

PIA U19 outputs commands for the reagent probe lift and swing functions, and monitors the reaction tray heater temperature and the reaction tray cover interlock switch.

2B3 Data Transfer Between Microprocessor and AC Motor Control Board

The main microprocessor communicates bidirectionally with the two PIAs (U13 and U19) on the AC Motor Control Board. The PIAs are selected by the 礙 via-A8-A14 as decoded by PROM U34. Each PIA receives 礙 address lines A0 and A1 (inverted by U35). When the PIA is selected, A0 and A1 determine the nature of the communication as specified in Table 2-1.

Data and instructions are transferred through data transceiver U36. During a WRITE operation, the-IOWC signal is delayed to make the clock pulses compatible with the AC Motor Control Board clock rate of 2 MHz.

Table 2-1 U13 & U19 DATA FLOW

TYPE OF TRANSFER	A1	A0	RD	WR
PORT A PIA → 祊	0	0	0	1
PORT A 礙 → PIA	0	0	1	0
PORT B PIA → 礙	0	1	0	1
PORT B 礙 → PIA	0	1	1	0
PORT C PIA → 礙	1	0	0	1
PORT C 礙 → PIA	1	0	1	0
STATUS PIA → 礙	1	1	0	1
COMMAND 礙 → PIA	1	1	1	0

The WR signal delay is initiated when the D7 bit of FROM U34 goes to logic 0. A low on the NAND gate (U33-4) input makes the output (U33-6) go high. The high is inverted by U35, and clears shift register U37. The shift register is then clocked at an 8-MHz rate by the CPU clock (CCLK) signal causing the outputs to go high as the register is clocked. The transfer acknowledge (XACK) signal then goes low and is directed back to the main 礙. The 礙 sends lOWC, and then waits for XACK. When XACK goes low, the 礙 continues program execution. Thus, the 礙 waits from the leading edge of IOWC until the leading edge of XACK, allowing more response time for the PIAs. Data is written into the appropriate PIA during the time between IOWC and XACK.

When data is read from the PIAs, a similar delay is created. When IORC goes low, the AC Motor Control Board data lines are transferred onto AD0-AD7 via transceiver U36. The read clock also clears shift register U37 via U33-3 and U33-6. The third CCLK pulse actuates XACK and completes the data transfer.

2B4 Sample Tray Motor On Command (Refer to Figure 2BFO1.)

To actuate the sample tray motor, U13 outputs a logic 1 pulse from PA2. The pulse is inverted by U16 and presets D flip-flop U27. The Q output of U27 goes high sending the output of NAND gate U3-3 low, to issue the SAMPLE TRAY MOTOR ON command from J5 pin 7 of the board. At the AC Motor & Sensor Control Board, the command closes switch S1 and directs 115 V ac to the tray motor. The tray then rotates to the next consecutive sample cup position.

The cutout in the sensor disk is now in position to enable light from the LED to be detected by the phototransistor. The phototransistor output goes from low to high and is input via J5 pin 5 to the AC Motor Control Board. The status signal is inverted by U25, and input to PB2 of U13, to inform the 礙 of tray status. The status signal also clocks U27 making the Q output low and the NAND gate U3-3 output high to shut off the motor.

2B5 Sample Probe Lift Motor Command (Refer to Figure 2BFO1.)

To actuate the sample probe lift motor U13 outputs a logic 1 pulse from PA4. If the motor command is to drive down, the output from PA5 of U13, the steering bit, is low. If the motor command is to drive up, the steering bit is high.

The high pulse from PA4 is inverted by U16 and presets D flip-flop U27. The Q output of U27 goes high sending the output of NAND gate U3-6 low, to produce the SAMPLE PROBE LIFT MOTOR command.

The low LIFT MOTOR command is issued from J5 pin 17 and is presented to the DC Motor & Sensor Control Board. Switch S1 on the DC Motor & Sensor Control Board closes on command and directs 24 V dc to the lift motor.

If, for example, the probe arm is to be driven down, the MOTOR ON command remains low until a cutout in the sensor disk is in position to allow light from the down sensor LED to strike the phototransistor. The phototransistor output goes from low to high and is input to the AC Motor Control Board via J5 pin 19. The high status signal is inverted by U25, and input to PB5 of U13 to inform the 磼 of probe status.

The low signal from U25 also causes the output of OR gate U38-6 to go low. The NAND gate U28 output will then go high, clock U27, and cause the Q output to go low. The SAMPLE PROBE LIFT MOTOR command then goes high and stops the motor.

2B6 Sample Probe Swing Motor Command (Refer to Figure 2BFO1.)

The probe swing motor ON command is generated when a logic 1 from PA3 is inverted by U16 and presets D flip-flop U15. The Q output of U15 goes high and actuates the PROBE SWING MOTOR ON command. The command is issued from J5 pin 27 of the AC Motor Control Board, and presented to the DC Motor & Sensor Control Board.

A probe position code is also issued from PA0, PA1, and PA7 of port A to comparator U26. The probe can be driven over any one of three positions: the oil reservoir, the sample cup, or the reaction tray dispense station. A logic zero programmed in only one of the PA0, PA1 and PA7 bits is compared with the three return sensor signals by comparator U26.

On receipt of the command, switch S3 on the sensor control board closes, and directs 24 V dc to the probe horizontal motor. The horizontal motor enables the probe arm to swing over each of the designated positions. The sensor assembly consists of a sensor disk attached to the horizontal motor, and three photodetectors. The photodetectors are stationed at points around the disk to detect when the probe is over the oil reservoir, the sample cup, or the reaction tray dispense stations.

For example, when the command is given to drive the sample probe over the sample cup, PIA U13 outputs a 101 code to the A inputs of comparator U26. The low PROBE SWING MOTOR ON command enables the horizontal motor to move the probe. When the cutout in the sensor disk is in position under the sample photodetector, a logic 1 status signal is sent back to the AC Motor Control Board. The signal is inverted and transferred to the B inputs of comparator U26, and PB1 of PIA U13. The position code at the B inputs of U26 now matches the position code at the A inputs of U26. Pin 6 of the comparator goes high and clocks D flip-flop U15. The Q output of U15 goes low and the NAND gate U3-8 output goes high to terminate the probe swing motor command and stop the motor.

2B7 Reagent Probe Motor On Commands

The reagent probe lift and swing command logic is identical to the sample probe lift and swing logic.

2B8 Reagent Tray Motor Control (Refer to Figure 2B-3.)

The reagent tray motor is controlled by the RAM Disk Board. Reagent tray position data are derived from an encoder wheel and sensor assembly. The encoder wheel has 24 rows of slots cut into it, each row representing a binary code for each tray position. Five binary bits are represented by the slots, the innermost slot being the least significant bit. (See Figure 2B-3.)

A sixth hole, located along the perimeter of the wheel, produces a strobe pulse for each tray position. This hole is smaller than the binary slots, and is situated toward the leading edge of each row of slots. The pulses produced by these strobe holes are used to shut off the reagent tray motor when the desired tray position has reached the aspirate station.

The encoder wheel is interposed between a photo emitter-detector array mounted on the reagent encoder PCB. Signals from the photodetectors are amplified and inverted by Darlington drivers. The photodetectors and Darlington drivers are powered by +5 V dc and -15 V dc from the RAM Disk Board.

To advance the reagent tray, the main CPU outputs address 0F5h, selecting PIA U21 and enabling input port B (see Table 2-2). A low on-IORC causes U21 to read the five tray position bits through port B, and place them on the data bus. Address 0F6h commands U21 to read the new tray position from the data bus, and load it into comparator U28 through U21 output port C.

Table 2-2 U21 DATA FLOW

ADDRESS	A1	A0	RD	WR	OPERATION	FUNCTION
0F4h	0	0	1	0	Data Bus → Port A	GO Command
0F5h	0	1	0	1	Port B → Data Bus	Read Tray Position
0F6h	1	0	1	0	Data Bus → Port C	Set New Position
0F7h	1	1	1	0	Data Bus → Control	Port I/O Configuration

0F4h is the GO command. Two positive pulses are issued from U21 ports PA6 and PA2. The pulse from PA6 clocks flip-flop U24 producing a high Q output (TRAY ENABLE). The PA2 pulse is inverted and sets the lower half of dual flip-flop U7, again producing a high Q output. These two high outputs are NANDed together to yield-TRAYMTR, which closes switch S1 on the AC Motor and Sensor Board.

The output of comparator U28 remains high until the tray position bits from the encoder assembly match the bits previously loaded into the comparator. When there is a match, the comparator output goes low. The low is inverted enabling AND gate U5, whose output will go high with the next encoder strobe. -TRAYMTR then goes high to shut off the reagent tray motor.

As noted earlier, the encoder wheel strobe holes are situated nearer to the leading edge of the tray position bit slots. This is to allow for coasting of the tray after the motor has stopped, ensuring that the tray comes to rest with the position code continuously available to the CPU.

When the tray cycle is completed, a high logic level is input to U21 port PB2. The CPU then issues an initialize (-INIT) signal to reset PIA U21 and flip-flop U24.

Figure 2B-3 REAGENT TRAY MOTOR CONTROL

2B9 ⊗ **RESET** (Refer to Schematic 108-C199.)

The ⊗ symbol on the AC Motor Control Board schematic is an active low signal that inhibits the a-c and d-c motors from energizing when system power is turned on. The initial logic low is produced when a system RESET signal is issued to D flip-flop U1 to clear it. A logic high is then issued from PIA U19 port PA6 to clock U1 and cause the Q output to go high.

2B10 Peripump Motor Control (Refer to Figure 2BFO2.)

The peripump is used to pump random access fluid from the reservoir to the probes.

To actuate the peripump motor, PIA U13 outputs a logic high signal from port PA6. The high is inverted by U16 and presets D flip-flop U15. The Q output of U15 goes high causing the output of NAND gate U3-11 to go low, which actuates the PERIPUMP MOTOR command at J5 pin 37. The command is presented to the AC Motor & Sensor Control Board. Switch S1 on the AC Motor & Sensor Control Board closes on command and transfers 115 V ac to energize the pump motor. The pump is energized for a period determined by a counter in the software.

The peripump sensor assembly consists of a sensor disk attached to the pump motor, and a photodetector. The sensor disk has four cutouts 90?apart.

Since the operating time for the pump is governed by the software, the sensor signals returned to the AC Motor Control Board are not read by the PIA, until requested by the software.

When the pumping time is near completion, the PIA is commanded to read the status signal from the pump sensor. The status signal from the sensor is inverted by the AC Motor Control Board, and input to port PB6 of PIA U13.

The high output from PA6 is then changed to a low, removing the preset condition on flip-flop U15. Flip-flop U15 is then clocked by the status signal from U14-12. The resulting low on the Q output of U15 turns off NAND gate U3-11, and stops the peripump motor.

2B11 Air Injection Timing Description (Refer to Figure 2BFO2 and Schematics 108-C199 and 108-C104.)

To improve reagent integrity between tests, and to aid in the mixing of reagents, approximately 13 air bubbles (followed by one extended bubble) are injected into the reagent stream during aspiration. The number of bubbles will vary according to the chemistry. Seventeen air bubbles, all of short duration, are injected into the reagent stream as the probe dispenses reagent into the reaction cuvette.

Each bubble is formed by trapping a slug of 5-psi air from the air pump between pinch valves 1 and 2. Pinch Valve 1 opens first, for 20 ms, and then closes to trap the air between both pinch valves. After a 50-ms delay, Pinch Valve 2 opens for 20 ms to release the trapped air to the reagent probe.

In the STANDBY mode, the Pinch Valve 1 solenoid is de-energized to pinch off the air line. The Pinch Valve 2 solenoid is energized at this time by the logic one input to U4 pin 7. The logic condition at U4 pin 7 is controlled by the output of port PC5 of PIA U13.

2B11.1 Circuit Description

Commands to Pinch Valves 1 and 2 are generated on the AC Motor Control Board. The circuit consists of PIA U13, a timing circuit with four NE 555 timers, and power driver IC U4.

During the air injection period, logic high output pulses (20 ms in duration) are issued from J7 pins 43 and 45. The pulses are optically coupled to two identical pinch valve driver circuits on the Air Injection Control Board. When a logic high pulse is input to either circuit, it causes the solenoid to energize, thus relieving pressure on the air tubing.

The air bubble injection period is initiated when the main microprocessor issues a command word to PIA U13 on the AC Motor Control Board. A logic zero enable signal is then issued from U13 port PC2, which, together with a low on WR, presets flip-flop U1. The Q output of U1 then goes high.

After the output of the enable signal, SYNC pulses are issued from U13 port PC4 every 200 ms. The SYNC pulses clock flip-flop U23-3 causing the Q output to go low and trigger timer U9. Timer U21 is triggered by the 10-ms output pulse from U9, and produces a 20 ms pulse. This output is directed to timer U10 to set up a 50-ms delay, and also is sent to inverter U12.

The 20-ms low pulses from inverter U12 are input to power driver U4 sending the U4 output high. During this period, pinch valve solenoid 1 is energized to release the air tube. Pressurized air enters the length of tubing between pinch valves.

Fifty ms later, timer U22 issues a 20-ms output pulse, which clocks U23 sending the Q output high. The OR gate (U24-6) output then goes high and is inverted by U14.

The low 20-ms signal from U14-8 is input to power driver U4, sending the output high. During this period the Pinch Valve 2 solenoid is energized, and the pressurized air is released to the reagent probe.

After the thirteenth bubble is injected into the reagent stream, there is a 0.5-ms delay. An extended air bubble command is then issued from PC5, whose output goes low for about 500 ms. The low clocks the Q output of U23-9 high, causing a high output from J7 pin 45, which enables Pinch Valve 2 to open. The extended air bubble ensures the dispensing of any reagent that may have entered the air line due to negative pressure buildup.

The air injection cycle is terminated by the U13 PC3 output going low to clear flip-flops U1 and U23.

2B12 AC Motor and Sensor Control Board Description (Refer to Schematic 108-C108.)

The AC Motor & Sensor Control boards are used in the sample and reagent tray, and peripump assemblies. The AC Motor & Sensor Control boards control the operation of the a-c motors by switching 115 V ac to the motors.

When a logic low MOTOR ON command is presented to the negative input of switch S1, the switch closes and allows 115 V ac to energize the associated a-c motor.

Jumper P1 connects E16 to E17 for 60-Hz operation, or E16 to E18 for 50-Hz operation.

2B13 DC Motor and Sensor Control Board Description (Refer to Schematic 108-C389.)

The DC Motor & Sensor Control board is used in the sample and reagent transfer mechanisms. The DC Motor & Sensor Control Board controls the operation of the d-c motors by switching 24 V dc to the motors.

NOTE

DC Motor & Sensor Control Board 108-B389-02 contains two identical motor and sensor control circuits: one for horizontal drive, and one for vertical drive. DC Motor & Sensor Control Board 108-B389-01 contains a third motor and sensor circuit for the horizontal drive of the ISE resample probe.

Refer to the vertical drive circuit shown in Schematic 108-C389. The following discussion applies to all three motor control circuits.

A logic low MOTOR ON command from inverter U2 turns on power driver U1. Switch S1 then closes and allows current to flow through forward biased diode D1, energizing the vertical d-c motor. Transistor Q1 is reverse based when the motor is operating.

When a MOTOR OFF command (logic high) is present at switch S1, the switch opens and cuts off the 24-V dc supply to the motor. Transistor Q1 then becomes forward biased and switches on, providing positive braking

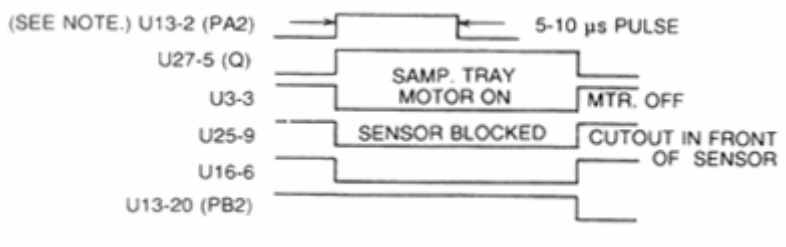
of the motor.

2B14 Air Injection Control Board Description (Refer to Schematic 108-C104.)

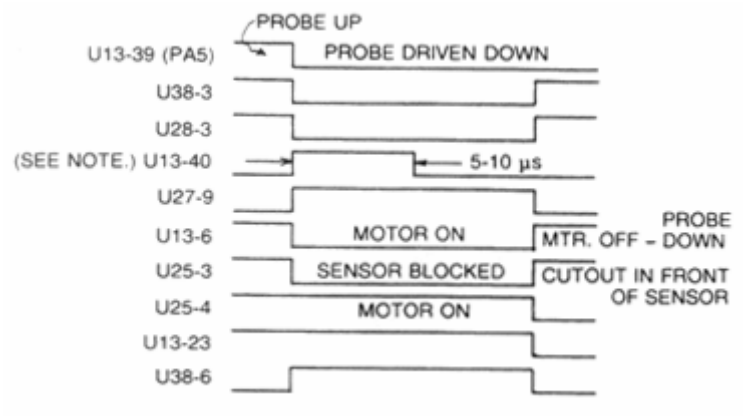
The air injection control board controls the operation of air injection pinch valve solenoids 1 and 2. A logic high air inject command from the AC Motor Control Board forward biases the optoisolator U1 LED turning it on. The detector output of U1 then goes low. The low is inverted by U2, which turns on the NPN transistor, opening a path to ground. Current then flows through the solenoid and pulls down the solenoid core, relieving pressure on the air tubing.

When the air inject command goes low, the transistor turns off, the pinch valve solenoid de-energizes, and the solenoid core returns to the up position, occluding the air tubing.

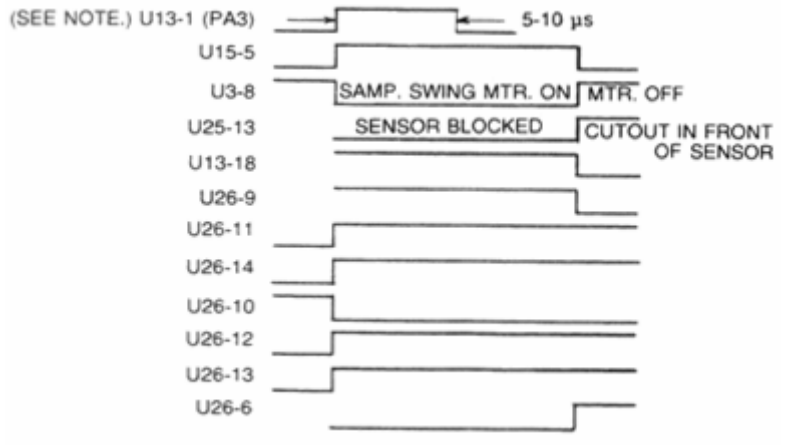
SAMPLE TRAY
MOTOR ON COMMAND LOGIC
AC MOTOR CONTROL BOARD



SAMPLE PROBE LIFT
MOTOR ON COMMAND LOGIC
AC MOTOR CONTROL BOARD



SAMPLE SWING
MOTOR ON COMMAND LOGIC
(probe swings from sample cup to reaction tray)
AC MOTOR CONTROL BOARD



NOTE:

SCOPE CONTROL SETTINGS TO DISPLAY 5 TO 10 社 PULSE
SLOPE ： POSITIVE

LEVEL : SLIGHTLY POSITIVE
SOURCE : DC
TRIG MODE : NORMAL
COUPLING : DC
TIME BASE : 5 祍/DIV
VOLTS/DIV : 5 VOLTS/DIV

Figure 2BFO1 SAMPLE TRAY AND SAMPLE PROBE LIFT AND SWING MOTOR CONTROL CIRCUITS

PERIPUMP MOTOR LOGIC
(1/4 TURN OF MOTOR)

AIR INJECT COMMAND LOGIC

Figure 2BFO2 PERIPUMP AND PINCH VALVE CIRCUITS

2C STEPPER MOTOR FUNCTIONS

The Technicon RA-XT system makes extensive use of stepper motors, which are all controlled by the Stepper Motor Controller Board (P/N 108-B189-03). High level commands to the Stepper Motor Controller Board come from the main 礙. Associated with each stepper motor is a Stepper Motor/Sensor Board. This board translates the logic level control signals that originate at the Stepper Motor Controller Board into the drive signals required by the stepper motor. The Stepper Motor/Sensor Board also transfers position sensor information from the sensor to the Stepper Motor Controller Board. The heat sink assembly associated with each stepper motor, supplies the drive current to the motor windings through series power resistors.

Functions controlled by stepper motors include:

- Sample and reagent PD pump vertical motion
- Reaction tray rotation
- Filter wheel rotation

2C1 Stepper Motor Description

A stepper motor is a permanent magnet motor that converts electronic signals into mechanical motion in discrete steps. Distributed around the stator of the motor are a series of windings (Refer to Figure 2C-1). When the direction of current in a winding is changed the motor output shaft rotates a specific angular distance or step. The windings must be turned on sequentially to go from one step to the next. The motor shaft can be driven in either direction, and can be operated at very high stepping rates. The motor is driven by a 24-V dc power supply, and is controlled by drive logic circuitry on the Stepper Motor Controller Board.

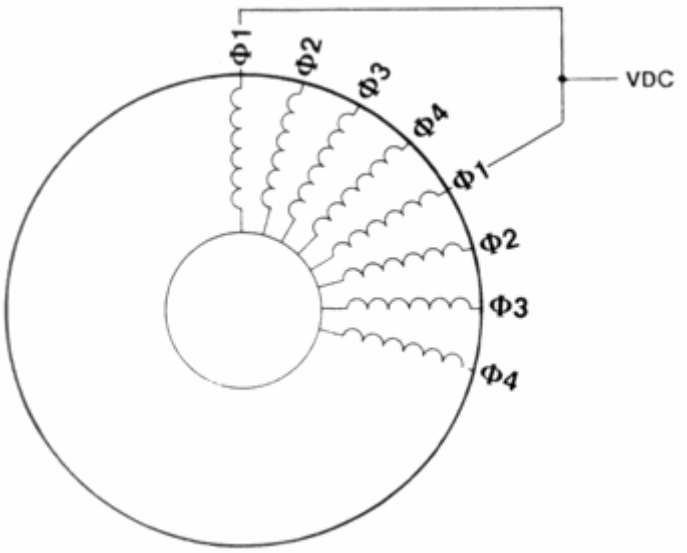


Figure 2C-1 STEPPER MOTOR WINDINGS

2C1.1 Basic Stepper Motor Operation

Figure 2C-2 shows a simple stepper motor with 90 degrees per step. There are four stopping positions. This is referred to as full-step operation, and is achieved by energizing a pair of windings to accomplish each step.

Figure 2C-2 FOUR STEPPER MOTOR POSITIONS - FULL STEP MODE

Figure 2C-3 EIGHT STEPPER MOTOR POSITIONS - HALF-STEP MODE

Figure 2C-3 shows a sequence for half-step operation. Half-step motion is achieved by energizing alternately a pair of windings and a single winding, as shown.

Figure 2C-4 illustrates a typical rotor and stator configuration for a 1.8-degree stepper. As shown, the motor consists of 8 stator poles with teeth machined into each stator pole and into the rotor. The number of teeth on the rotor and the stator determines the step angle (degree of rotation per step).

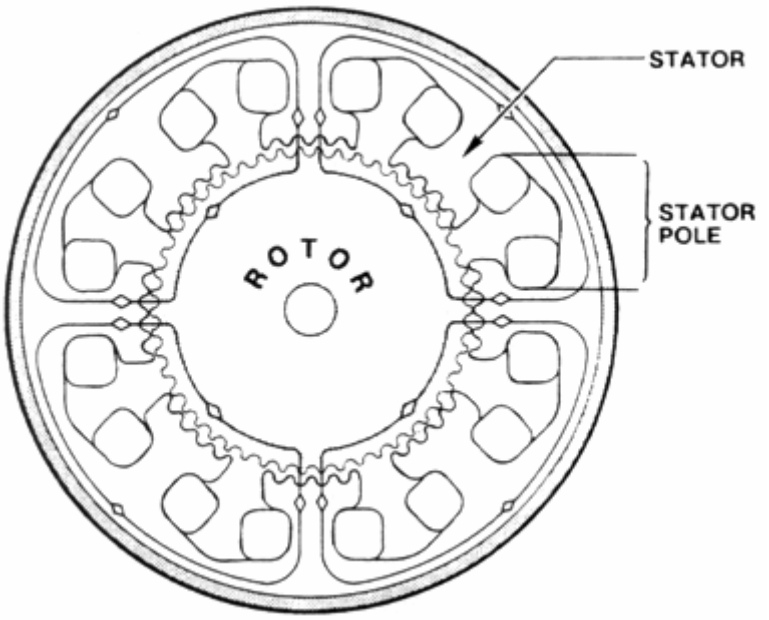


Figure 2C-4 STEPPER MOTOR

The filter wheel and the reagent and sample positive displacement pump stepper motors are operated in the full-step mode. The filter wheel stepper motor has 200 steps per revolution with a step angle of 1.8 degrees. The reagent and sample stepper motors have 48 steps per revolution with a step angle of 7.5 degrees.

The reaction tray stepper motor is driven in the half-step mode with 400 steps per revolution and a 0.9-degree step angle.

As shown in Figure 2C-5, full-step operation occurs when two of the four motor windings are energized for each step. This method provides more driving power than the half-step mode.

As shown in Figure 2C-6, half-step operation occurs when, alternately, one winding and then two windings are energized. The advantages of operating in this mode are finer resolution and greater speed.

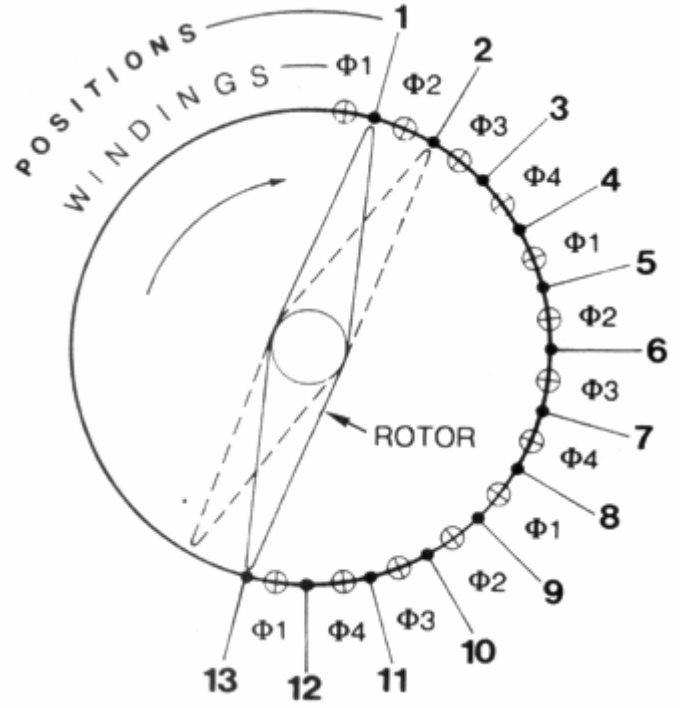


Figure 2C-5 STEPPER MOTOR FULL-STEP OPERATION

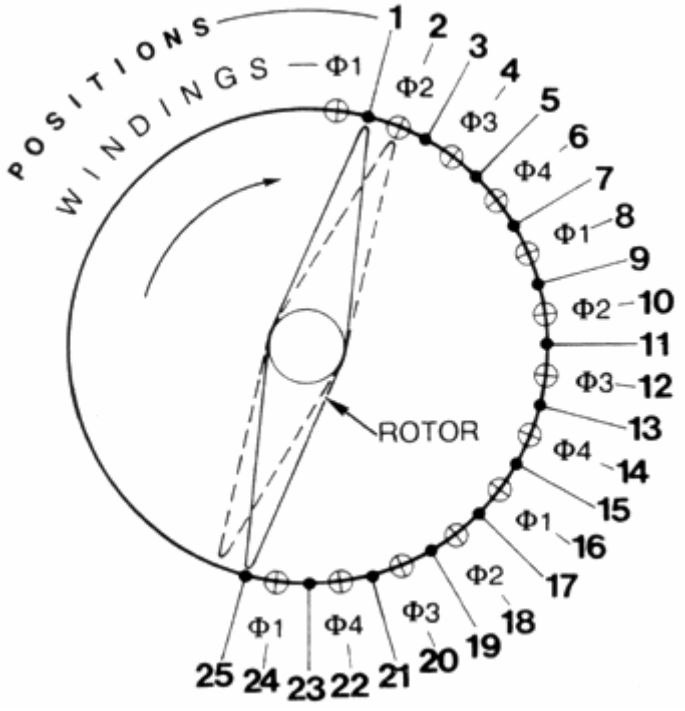


Figure 2C-6 STEPPER MOTOR HALF-STEP OPERATION

2C1.2 Basic Stepper Motor Characteristics

Residual Torque

When power to the motor is turned off, the output shaft of the motor is held in position by the residual torque. Residual torque results from the permanent magnetic flux acting on the stator pole.

Holding Torque

Holding torque maintains the output shaft in position by energizing one or both windings when the motor is not stepping. Holding torque is much greater than residual torque.

Stepper Motor Damping

Damping of the motor is required to prevent oscillations as the motor stops. The oscillations are caused by variations in load resistance, which occur as the motor slows down. Damping can be achieved by mechanical or electronic means.

Transient Voltage Suppression

To suppress transient voltages, shunting diodes CR1 through CR8 are incorporated into the stepper motor switch circuitry on each Stepper Motor/Sensor Board (described in section 2C8). Transient voltages are generated as current is switched through the windings during stepping. If not suppressed, these transient voltages can damage the motor.

2C1.3 Stepper Motor Supply Voltage

As shown in Figure 2C-7, the +24-V dc supply voltage to the stepper motor is routed through the heat sink assembly. The large resistors on the heat sink assembly improve motor performance, and protect the power supply from burning out due to the large current requirements of a stepper motor.

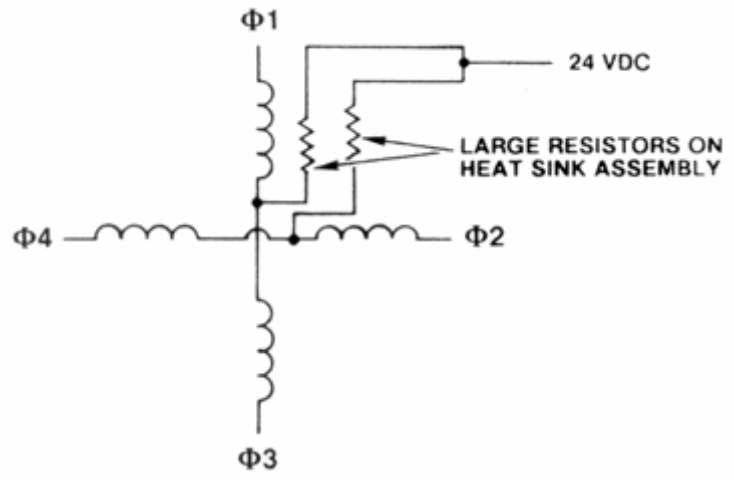


Figure 2C-7 SUPPLY VOLTAGE TO STEPPER MOTOR WINDINGS

2C2 Stepper Motor Homing

The starting position of the stepper motor is determined by the home position sensor. The home sensor is located on the device the motor is driving. If the home sensor is not aligned properly, or fails to function, the CPU cannot determine the current position of the device driven by the stepper motor.

2C2.1 Reaction Tray Home

The home sensor for the reaction tray indicates when cuvette number one is in position to accept reagent. When in the home position, the stepper motor is aligned at a predetermined winding pattern specified by the software. Once sampling has started, the reaction tray does not return to the home position until all 100 cuvettes have been assayed, or a new tray is placed on the system. The reaction tray sensor disk has four cutouts positioned 90 degrees apart. The deepest cutout indicates when the tray is at the home position. The 90-degree cutouts indicate 90-degree rotation of the disk as the cutouts pass in front of the sensor, i.e., when cup 1, 25, 50, or 75 is in position to receive reagent.

2C2.2 Filter Wheel Home

The filter wheel home position indicates that filter number one is in the measurement position. The home position is detected when the cutout in the edge of the filter wheel is positioned under the sensor device. In the home position, the stepper motor is aligned at a winding pattern determined by the software.

During a read period, a cuvette is positioned in front of the colorimeter for a period of 120 ms. Eighty milliseconds of this period are used to position a filter in the colorimeter light path. The filter wheel sequences to the proper filter as each cuvette is positioned at the colorimeter read station. After reading 43 cuvettes, the filter wheel returns to the home position and waits for the next read period.

2C2.3 Positive Displacement Pump Home

The sample and reagent positive displacement pumps are at the home position when the plunger is at the top of the syringe. At this point, the stepper motors are positioned at a specific winding pattern determined by the software. After each dispense cycle, the plungers return to their home positions.

2C3 Stepper Motor Driven Devices

2C3.1 Reaction Tray

The reaction tray is belt driven by the stepper motor as shown in Figure 2C-8. The belt drive ratio between the stepper motor and reaction tray is 4:1. With every four revolutions of the stepper motor, the tray will rotate one complete revolution. One revolution of the stepper motor requires 400 half steps. The reaction tray contains 100 cuvettes; each cuvette is 16 half steps wide. Therefore, one revolution of the reaction tray requires 1600 half steps. Table 2-3 illustrates stepper motor revolutions versus reaction tray rotation.

Table 2-3 STEPPER MOTOR REVOLUTIONS VS. REACTION TRAY ROTATION

STEPPER MOTOR		REACTION TRAY	
Revolutions	Half Steps	Rotation	No. Cups
one	400	90	25
two	800	180	50
three	1200	270	75
four	1600	360	100

Figure 2C-8 REACTION TRAY 90° FROM HOME

2C3.2 Filter Wheel

The filter wheel also is belt driven by a stepper motor as shown in Figure 2C-9. The belt drive ratio between the stepper motor and the filter wheel is 1:1. The stepper motor takes 200 full steps per revolution, and rotates the shortest distance between filters in either a CW or CCW direction. There are eight filter positions. Table 2-4 indicates the number of steps the motor must drive to position each filter in the colorimeter light path.

Table 2-4 FILTER POSITIONING

FILTER POSITION	FULL STEPS FROM HOME
1	200
2	25 CW
3	50 CW
4	75 CW
5	100 CW
6	75 CCW
7	50 CCW
8	25 CCW

Figure 2C-9 FILTER WHEEL ROTATED TO PLACE FILTER 2 IN READ POSITION

2C3.3 Positive Displacement Pumps

The sample and reagent positive displacement pumps are driven by rack and pinion assemblies coupled to stepper motors as shown in Figures 1D-16 and 1D-17. (Newer systems are lead screw driven.) Each stepper motor takes 48 full steps per revolution. The stepper motors are commanded to drive in quarter turn (12-step) increments. To move the plunger from the bottom of the syringe to the top, the stepper motor must drive 1050 full steps. Ten steps of the stepper motor equal a 1% displacement of the volume within the syringe.

2C4 Stepper Motor Control Circuits (Refer to Schematic 108-C189.)

A stepper motor operation is initiated when the main 礙 addresses the chip select PROM on the Stepper Motor Controller Board. The PROM decodes the address and selects the 8741A CPU requested by the main 礙. The Stepper Motor Controller Board contains four 8741A CPUs. Each CPU controls one of the three stepper motor driven devices described in Section 2C3.

When a particular 8741A CPU has been selected, it is then able to accept and transfer data and instructions from the main 礙. The internal program in the selected CPU enables it to issue the control commands to the Stepper Motor/Sensor board. The 8741A CPU also provides stepper motor status to the main 礙 on request.

On receiving the logic level phase commands, the Stepper Motor/Sensor Board switches the drive voltage through the board to energize the appropriate ϕ1, ϕ2, ϕ3, and ϕ4 windings in the stepper motor.

2C4.1 Sensor Assemblies

The sensor assemblies for the reagent and sample positive displacement pumps indicate to the 8741A CPU when the pump plunger is at the home or topmost position.

The filter wheel sensor assembly indicates to the CPU when the home or number one filter is in the read position.

The reaction tray sensor assembly consists of two photodetectors, and a sensor disk with cutouts every 90? around the disk. One sensor detects 90?rotations of the sensor disk. The other sensor detects the home or cuvette number one position. The home position cutout on the sensor disk is cut deeper into the disk than the 90?cutouts. Thus, the sensor can distinguish between a 90?cutout and the home position cutout.

2C5 Stepper Motor Functional Diagram

Figure 2CF02 is a functional diagram showing how the filter wheel stepper motor is controlled. This diagram is applicable to the other stepper motors, however, the sensor configuration varies from motor to motor.

Movement of the motor is initiated by the 礙 via commands sent to the 8741A CPU. For the filter wheel, the 礙 sends two types of commands. One type of command sends the filter wheel to the home postion, while the other type sends the filter wheel to one of the other positions. There are actually seven commands, corresponding to the seven filter positions (plus home). These commands are eight bit words. The four most significant bits are 0010 (go to position X). The four least significant bits specify the filter wheel destination. This command is abbreviated 2X, where X is the destination. This command format is used for various commands such as slew the reaction tray (X cup positions), move the positive displacement pump stepper motor (X steps), etc.

When the command is received by the 8741A CPU, the appropriate stepper motor control signals are generated. The 8741A produces four stepper motor control signals: ϕ1, ϕ2, ϕ3, and ϕ4. These signals are buffered and sent to the Stepper Motor/Sensor Board.

The Stepper Motor/Sensor Board receives the logic level ϕ1 through ϕ4 signals and translates them into the signals required to drive the motor. The stepper motor is driven by logic lows on the ϕ1 through ϕ4 motor inputs. The other end of the stepper motor coils receive the proper drive voltages from the heat sink assembly.

The filter wheel sensor produces a logic level signal that indicates whether or not the filter wheel is in the home position. The signal from the sensor is sent through the Stepper Motor/Sensor Board to the Stepper Motor Controller Board. The 8741A CPU reads the sensor signal to determine the filter wheel position.

2C6 Stepper Motor Controller Board Description (Refer to Figure 2CFO1.)

The Stepper Motor Controller Board provides the ϕ1, ϕ2, ϕ3, and ϕ4 logic level control commands to operate the reaction tray, the filter wheel, and the reagent and sample positive displacement pump stepper motors.

The Stepper Motor Controller Board is the communication link between the main 磯, which initiates a specific motor drive sequence, and the stepper motors.

To communicate with the stepper motors the Stepper Motor Controller Board uses four 8741A single chip microcomputers. Each CPU has its own 1k of EPROM, 64 bytes of static RAM, I/O ports, and CPU with control timing.

Each CPU is assigned a particular stepper motor driven device to control. For troubleshooting purposes the 8741A CPU for the reaction tray and the ones for the positive displacement pumps may be interchanged.

2C6.1 Program Selection of 8741A CPU

The main 磯 program determines the selection of the desired 8741A CPU by outputting the address number for the desired CPU. The address is decoded by PROM U28 on the stepper motor controller board (see Schematic 108-C189, Sheet 2).

After an 8741A CPU is selected, the internal 8741A program takes control. The 8741A communicates with the main 磯 through an internal data bus buffer, I/O register, and an 8-bit DBB status register with four bits user definable. The four status bits are:

F1 = 1	Main 磯 requests status
F1 = 0	Main 磯 requests or transmits data
F0 = 1	Stepper motor in motion.
F0 = 0	Stepper motor stopped.
IBF	(Input Buffer Full)
IBF= 1	Main 磯 has sent data or an instruction to be acted upon.
OBF	(Output Buffer Full)
OBF = 1	This bit is an error flag. It indicates that the data received from the main 磯 could not be successfully processed.

As dictated by the 8741A internal program, the data words for the stepper motor phases are issued through I/O port 2. The active high phase command from the 8741A is sent to the NAND gate portion of power ICs U7 and U8 (75461s). The low output of the gate turns off the transistor portion of the IC, driving the collector high to produce the ϕ1, ϕ2, ϕ3, and ϕ4 logic level command signals. The commands are presented to the Stepper Motor/Sensor Board.

2C6.2 Data Transfer Between Microprocessor and Stepper Motor Controller Board

The main 磯 transfers data and instructions to the Stepper Motor Controller Board through an 8-bit data bus. Four control lines (RD, WR, CS, and A0) are used by the main 磯 to execute the exchange of data or instructions. A logic 1 in the A0 bit position indicates to the interface that the 磯 is requesting status. A logic 0 in the A0 bit position indicates that the 磯 is requesting or transmitting data. The logic level of the RD or WR signals from the 磯 indicate the direction of data flow on the data bus. The WR signal is low when the stepper motor drive data are sent to the Stepper Motor Controller Board. The RD signal is low when status or data are transferred to the 磯. Data and instructions are transferred through data transceiver U29 on the Stepper Motor Controller Board. Table 2-5 indicates the condition of control lines when data is input or output.

Table 2-5 8741A DATA FLOW

INSTR	CS	RD	WR	A0	OPERATION	CPU 8741A REGISTER
IN	0	0	1	1	READ	STATUS → 礙
IN	0	0	1	0	READ	DBB → 礙
OUT	0	1	0	0	WRITE	礙 → DBB

During a read or write operation, the -IOWC or -IORC signal is delayed to make the clock pulses compatible with the Stepper Motor Controller Board clock rate of 2 MHz.

The 礙 actuates -IOWC or -IORC and waits for -XACK. By delaying -XACK, the stepper motor board slows the 礙. -XACK is produced by shift register U11. The Q2 output of U11 is transferred onto -XACK by tri-state driver U10-13. This tri-state driver is enabled by U14-6 only when PROM U28 output 7 is low (and -IOWC or -IORC is present). When a stepper motor IC is not being addressed, PROM U28 output 7 is high, and the Stepper Motor Controller Board does not control -XACK.

The output of NAND gate U14-6, which enables tri-state driver U10, also enables shift register U11. Just before -IORC or -IOWC is enabled, the high U14-6 output clears U11 via inverter U12-8. When the -IORC or -IOWC signal goes low the clear is removed, enabling U11. The U11 clock is the 8-MHz -CCLK signal. After two -CCLK cycles, U11 enables -XACK, completing the delay operation.

2C6.3 Stepper Motor Commands for the Reaction Tray and PD Pumps

Command	Description
1X	Index stepper motor the number of cup positions specified by X.
2X	Slew stepper motor the number of cup positions specified by X.
3X	Home the motor. Used for all stepper motors except the reaction tray.
4X	Operate the motor in the full step mode. This is the default mode when no other mode is given. X is not used.
5X	Operate the motor in the half step mode. X is not used
6X	Step time setup. Motor speed is increased or decreased by adjusting the step time period in increments of 0.08 ms, which is the interrupt timing interval of the interface.
7X	Not used
8X	Turn the motor the number of quarter turns specified by X. This command is used for the peripump motors, which only operate in quarter turn increments.

2C6.4 Stepper Motor Commands for the Filter Wheel

Command	Description
1X	Send filter wheel to the home position. This position will be the most frequently used filter. X is not used
2X	Go to filter position specified by X.

2C7 Heat Sink Assembly (Refer to Schematic 108-C162 and Figure 2CFO1.)

The heat sink assembly supplies the drive currents for the reaction tray, filter wheel, and sample and reagent P.D. pump stepper motors. Each drive circuit on the heat sink assembly is identical except for the quantities and values of current limiting resistors. The drive currents to the ϕ1 through ϕ4 stepper motor windings are supplied through the current limiting resistors.

2C7.1 Circuit Description

+ 24 V dc to the filter wheel drive circuit is distributed as follows:

a) +24 V dc is routed through pin 3 of J2 and supplies 24 V dc to voltage regulator VR1 on the Stepper Motor/Sensor Board.

b) + 24 V dc NET is supplied through pin 1 of J2 and is directed to noise suppression diodes CR1 through CR8 on the Stepper Motor/Sensor Board.

c) + 24 V dc is dropped to a lower voltage across current limiting resistors R3 and R4, and R13 and R14 when a motor winding is turned on, and directed through pins 5 and 7 of J2, where it is routed to the ϕ1, ϕ2, ϕ3, and ϕ4 stepper motor windings.

d) The 24-V d-c return from the Stepper Motor/Sensor Board is directed through the heat sink assembly to the 24-V d-c return line.

2C8 Stepper Motor/Sensor Board (Refer to Schematic 108-C197 and Figure 2CFO1.)

The Stepper Motor/Sensor Board controls the turning on and off of the stepper motor drive currents through four transistor switches.

The transistor switches are turned on and off by the ϕ1 through ϕ4 logic level command signals from the Stepper Motor Controller Board.

The Stepper Motor/Sensor Board also transfers the +5-V d-c supply voltage from the Stepper Motor Controller Board to the photo sensor assembly. The status signal from the sensor assembly is directed back to the Stepper Motor Controller Board through the Stepper Motor/Sensor Board.

The Stepper Motor/Sensor Board contains four identical switching circuits for controlling the motor windings. Plus 24 V dc is supplied to transistors Q1 through Q4 and voltage regulator VR1. The voltage regulator provides a +5-V d-c output, which is supplied to opto-isolators U1 and U2 and inverter U3 The +5 V dc supplied to these devices is isolated to suppress any noise interference that might be picked up from the motor circuit.

2C8.1 Circuit Description

The logic level commands to turn on the ϕ1 and ϕ2 windings are applied to pins 13 and 15, respectively, on the Stepper Motor/Sensor Board, and directed to opto-isolators U2 and U1. (The opto-isolators optically decouple any noise transients that may be generated by the motor circuit from entering logic level control circuitry.) When the logic level commands are high, the LEDs are forward biased. The light emitted by the LEDs is detected by the optical sensors, driving the outputs low.

The low outputs from U2 and U1 are inverted by buffer U3 to turn on transistors Q2 and Q3. The stepper motor drive current from the heat sink assembly is then drawn through the ϕ1 and ϕ2 windings in the motor. With transistors Q2 and Q3 turned on, current flows to the 24-volt return and drives the motor one step.

Diodes CR3 and CR4, also connected to the 24-volt return, suppress any voltage spikes over 24 V dc. When the voltage due to inductive rotation of the rotor starts to go beyond 24 V dc, diodes CR3 and CR5 become forward biased, and inhibit any voltage increase. Circuit operation is the same for the ϕ3 and ϕ4 windings.

2C8.2 Reaction Tray Stepper Motor Half Step Operation

The half-step mode of operation requires that two windings, and then one winding, alternately energize as shown in the winding pattern diagram (Figure 2C-10). The starting position of the stepper motor rotor is at the motor home winding pattern. The rotor goes through eight steps before returning to the motor home winding pattern. The winding pattern sequence is repeated as the stepper motor rotor cycles through a 360?revolution. (The stepper motor home winding pattern is not to be confused with the home position of the reaction tray, which occurs only when the home cutout on the sensor disk is positioned in front of the home photodetector.)

Figure 2C-10 STEPPER MOTOR WINDING PATTERNS

Figure 2C-11 SIMPLIFIED STEPPER MOTOR CIRCUIT

Figure 2C-11 is a simplified stepper motor circuit diagram showing how current from the heat sink assembly is applied when a motor winding is on or off. Steps 1, 3, 5, and 7 as shown in the winding pattern diagram have three windings off (indicated by a 0), and one winding on (indicated by a 1). Step 7 of the pattern will be used as an example to show how the current is supplied to the windings. In this winding pattern, the ϕ3 winding is on, and the ϕ1, ϕ2 and ϕ4 windings are off. The voltage on the ϕ2 and ϕ4 windings reads about 24 V dc (at E7 and E8), since no current is drawn through the current limiting resistors in the heat sink circuit. The voltage on the ϕ1 winding reads about 2.6 V dc at E6, since the current through the current limiting resistors in the heat sink circuit is shared with the ϕ3 winding. The ϕ3 winding is on, and reads about 1.0 V dc at E5. See Figure 2CF01 for detailed winding pattern voltages.

Any time two windings are on and two are off, the windings that are on read about 1.0 V dc, and those windings that are off read about 2.6 V dc.

2C8.3 Filter Wheel and PD Pump Full-Step Operation

In the full-step mode, two windings are on and two are off as shown in the winding pattern diagram (Figure 2C-10). The stepper motor rotor starts at the motor home winding pattern, the rotor passes through four steps before returning to the motor home winding pattern. This sequence is repeated as the rotor cycles through a 360?rotation. The motor home winding pattern is not to be confused with the home position of the device it is driving. The voltage read at the windings that are on in the filter wheel stepper motor is about 1.0 V dc, and 2.6 V dc for those windings that are off.

The voltage read at the P.D. pump windings that are on is about 0.8 V dc and 6.1 V dc for windings that are off. The difference in voltage for the windings on the P.D. pumps and those for the filter wheel stepper motor windings is due to the electrical characteristics of each motor.

Voltage measurements can be taken at terminals E5, E6, E7, and E8 on the Stepper Motor/Sensor Board for the corresponding motor.

Table 1

	ϕ1 (E6)	ϕ2 (E7)	ϕ3 (E5)	ϕ4 (E8)
Motor Home Position	0 (2.8 V)	1 (1.1 V)	1 (1.1 V)	0 (2.6 V)
1	0 (24 V)	1 (1.1 V)	0 (24 V)	0 (2.7 V)
2	1 (1.1 V)	1 (1.1 V)	0 (2.7 V)	0 (2.8 V)
3	1 (1.1 V)	0 (24 V)	0 (2.7 V)	0 (24 V)
4	1 (1.1.V)	0 (2.7 V)	0 (2.7 V)	1 (1.2 V)
5	0 (24 V)	0 (2.7 V)	0 (24 V)	1 (1.1 V)
6	0 (2.7 V)	0 (2.7 V)	1 (1.1 V)	1 (1.2 V)
7	0 (2.6 V)	0 (24 V)	1 (1.0 V)	0 (24 V)
Motor Home Position	0 (2.8 V)	1 (1.1 V)	1 (1.1 V)	0 (2.6 V)

Table 2

	ϕ1 (E6)	ϕ2 (E7)	ϕ3 (E5)	ϕ4 (E8)
Motor Home Position	0 (2.7 V)	1 (1.2 V)	1 (1.2 V)	0 (2.7 V)
1	1 (1.3 V)	1 (1.2 V)	0 (2.8 V)	0 (2.7 V)
2	1 (1.2 V)	0 (2.8 V)	0 (2.7 V)	1 (1.3 V)
3	0 (2.8 V)	0 (2.8 V)	1 (1.2 V)	1 (1.3 V)
Motor Home Position	0 (2.7 V)	1 (1.2 V)	1 (1.2 V)	0 (2.7 V)

NOTE

- Motor home position is indicated by 揌OME?displayed on the CRT.
- 0 = winding OFF.
- 1 = winding ON.
- Voltages may vary a few tenths of a volt +/- from those indicated in the tables.

Figure 2CFO1 FILTER WHEEL STEPPER MOTOR CIRCUITS

2D COLORIMETER (Refer to Figure 2D-1.)

The colorimeter is an optical device that measures the amount of light absorbed by the color developed in a sample or blank cuvette.

The colorimeter is mounted on the side of the reaction tray module. During a read period, each sample cuvette is positioned in front of the sample photodetector for 120 ms. About 80 ms of the 120-ms period is used for positioning the filter wheel. About 40 ms of the read period is used to read the reference and sample values. To minimize drift, the colorimeter optics are heat soaked in an airbath temperature controlled to 30癈 or 37癈 ?癈.

The colorimeter consists of a tungsten halogen lamp operated at 7.2 V dc while the system is in the operate mode. To prolong lamp life, the lamp voltage is reduced to 5.0 V dc when the system is in the STANDBY mode. A beam splitter and various lenses are used to focus and direct the light beam to the reference and sample photodetector boards. A stepper motor driven filter wheel containing eight filter positions is used to select a particular wavelength of light for the applicable methodology. The filter wavelengths are: 340 nm, 380 nm, 405 nm, 500 nm, 550 nm, and 600 nm. One filter position is used for dark current, and the remaining position is unassigned.

As a sample cuvette is rotated into position, the light from the source lamp is focused onto the selected filter. The filter allows only a particular wavelength of light to pass through. Light from the filter is split by the beam splitter, and sent along reference and sample optical paths.

As the reaction mixture in the sample cuvette darkens, the amount of light striking the sample photodetector decreases proportionally. The proportional decrease is compared with the constant output of the reference photodetector.

The light striking the sample and reference photodetector is transformed into electrical signals that are input to operational amplifiers. The operational amplifiers boost the signals to measurable levels for use by circuits on the A/D Converter Board.

Figure 2D-1 FUNCTIONAL DIAGRAM OF COLORIMETER

2D1 A/D Converter Board Description (Refer to Figure 2DFO1 and Schematic 108 - C146.)

The A/D Converter Board transforms the colorimeter analog sample and reference voltages into frequency equivalents. A self-contained module, the A/D converter is mounted on the Data Acquisition Board. Analog switch U2 and two switches internal to U3 (S2 and S3) are not used.

The reference and sample analog signals are coupled sequentially to analog switch U3. The reference signal is a measurement of the total amount of source light striking a photodetector. The sample signal is the percentage of source light striking a photodetector after passing through a cuvette containing sample (or blanking reagent).

U5 (see Schematic 108-C146) is a dual 1-of-4 decoder. The input to U5 pins 15 and 1 is the FT1 signal from the Data Acquisition Board. The state of FT1 selects decoder 1 or 2 (within U5). When U5 decoder 1 is enabled, one of the 1Y0-1Y3 lines goes low. When U5 decoder 2 is enabled, one of the 2Y0-2Y3 lines goes low. In our application, decoder 1 is enabled when the A/D module is used.

The state of the U5 A and B inputs controls which output line (1Y0 - 1Y3) goes low. The A and B inputs receive FT2 and FT3 from the Data Acquisition Board.

U5 outputs 1Y0-1Y3 are provided to analog switch U3. When 1Y0 is low, the sample analog signal is transferred to the U3 output. When 1Y1 is low, the reference analog signal is transferred to the U3 output. In our application, 1Y2 and 1Y3 do not go low. Table 2-6 shows how FT1, FT2, and FT3 select the sample or reference analog signal. The selected analog signal is converted to a frequency by U1.

Table 2-6 SAMPLE/REFERENCE CHANNEL SELECTION

FT1	FT2	FT3	1Y0	1Y1	SELECTION
1	0	0	0	1	Sample
1	0	1	1	0	Reference

The FT1 signal goes high at the beginning of each 16.5-ms read period. (There is a 16.7-ms reference read period, followed by a 16.5-ms sample read period.)

The V/F converter is capable of reading analog input voltages from 0 to 10 V dc. A 10-Volt input signal is converted to an output frequency of 1 MHz. Input voltages are scaled to 100 kHz/Volt.

The dark current offset frequency of 5.745 kHz ?10% is produced by using precision resistors R1, R2, and R3 at the input of the converter.

NAND gate U4 buffers the output frequencies to produce negative going pulses having a width of 0.5 μs ?0.1 μ s. The reference and sample signals are output through terminal E6 of the board. Amplifier AR1 may be nulled by installing plug P1 between E14 and E16. Resistor R4 is then adjusted to make the voltage measured at TP1 zero volts.

2D2 Data Acquisition Board Description (Refer to Figure 2DFO1 and Schematic 108-C186.)

The Data Acquisition board accumulates the counts for the sample and reference signals from the A/D converter Board. The counts are retained in digital form until called for by the 礙.

The A/D Converter Module (108-B146) and two programmable peripheral devices are mounted on the board. The peripheral devices are PIA U9 (8255) and programmable interval timer U10 (8253).

The 礙 communicates with the Data Acquisition Board through PIA U9 and PIT U10. The PIA consists of a data bus buffer, read/write control logic, and 3 ports. A control word from the 礙 board, sets up the ports in one of 3 modes of operation. On PIA U9, port A is an output, PBO of port B is an input, and port C is not used.

PIT U10 consists of a data bus buffer, read/write control logic, command register, and three independent 16-bit down counters.

Counter Zero counts the transitions of the 0 to 1 MHz reference signal from the A/D converter board for one period of the power line frequency (16.6 ms for 60-Hz systems, 19.5 ms for 50-Hz systems). Counter One counts the transitions of the 0- to 1-MHz sample signal from the A/D Converter Module, also for one period of the power line frequency.

Counter Two acts as a time base counter driven by a 1-MHz frequency to produce either the 16.5-ms count gate for 60-Hz systems, or the 19.5-ms count gate for 50-Hz systems. The U10 GATE 2 input (pin 16) is high for the 16.6-ms or 19.5-ms period. The Counter Two carry output (U10 pin 17) is used to time the length of the FT1 control line to the A/D Converter Module.

The accumulated counts are derived in the following manner:

- **For domestic systems - 100 kHz x 0.0166 s = 1660 counts/volt.**
- **For international systems - 100 kHz x 0.0195 s = 1951 counts/volt.**

2D2.1 Selection of PIA U9 or U10 by Microprocessor

The main 礙 program selects the desired device by outputting the address number for either PIA U9 or PIT U10 to PROM U7 on the Data Acquisition Board. The XACK signal is delayed by U4 and associated circuitry.

2D2.2 Circuit Description (Refer to Figure 2DFO1.)

As described in Section 2D1, the A/D Converter Module changes the colorimeter sample and reference voltages into frequencies equivalent to the sample and reference analog signal levels. The sequential reference and sample frequencies are input to PIT U10 on the Data Acquisition Board by their read time commands.

To initiate the 40-ms read time for each cuvette, the following occurrences take place on the Data Acquisition Board:

1. Counter Zero and Counter One (internal to U10) are loaded with 1担.
2. CLEAR from port PA6 on U9 is brought to a logic 0, and the ENABLE line from PA7 and the TWO WORDS line from PA1 on U9 go high.
3. The high levels at the input pins to NAND gate U12 cause output pin 6 to go low. The low output is then inverted, and allows the 1-MHz clock signal to clock the time base counter (Counter Two).
4. The high logic signals at the input pins to NAND gate U11 cause output pin 12 to go low. The low output is then inverted to produce the Gate 0 input to U10.
5. With the Gate 0 input high, the reference frequency from the A/D Converter Board clocks down Counter Zero (internal to U10) for the 16.5-ms count gate.
6. Counter Two continues decrementing as it is driven at the 1-MHz frequency. Upon underflow, the output of Counter Two rises and clocks flip-flop U15-3, which terminates Counter Zero. (The gate to Counter Zero is inhibited by pin 1 of U11 going from high to low.)
7. Upon termination of Counter Zero, the reference count, which is equivalent to the reference voltage, is retained in Counter Zero.

8. After a delay of about 100 衽 by one shot U19, Counter Two is retriggered and again acts as a time base counter.
9. After Counter Two is retriggered, the input to gate U11-3 is high, changing the output U116 to low. The low output is then inverted and produces the Gate 1 input to U10.
10. With Gate 1 high, the sample frequency from the A/D converter clocks down Counter One of U10 for the 16.6-ms period.
11. Upon termination of the 16.6-ms count, the sample count, which is equivalent to the sample voltage, is retained in Counter One.
12. One microsecond later, D flip-flop U15-3 is clocked, the Q output goes high and clocks flip-flop U15-11.
13. When the Q output of U15-9 is high, NAND gate output U18-6 is low, and OR gate output U18-8 is high, activating the FINAL INHIBIT command to pin 18 of PIA U9 (PB0). The high on pin 18 informs the 礹 that both the reference and sample words reside in the programmable interval timer (U10).
14. The data is retained in the counters until called for by the 礹. The 16-bit contents of U10 interval Counter One or Two are transferred to the 礹 as two 8-bit words.
15. A CLEAR signal is issued from the 礹 to deactuate the ENABLE and TWO WORD lines.

2D2.3 Sample and Reference Read Time Commands

The Data Acquisition Board also provides the read time commands for the reference and sample signals. The commands are issued to dual 2-to-4 line decoder U5 on the A/D Converter Module. The commands are generated as follows.

a) Bits PA3, PA4, and PA5 of PIA U9 are set to a logic 0.

b) The PA5 output is set to logic 1 by inverter U16-12, and becomes output FT3.

c) The low on PA4 becomes output FT2

d) The PA3 output is coupled to input 2 of OR gate U14. Input pin 1 of U14 is a logic 1 for the 16.5-ms reference count gate. At the termination of the reference count, pin 1 goes low for the 16.5-ms sample count gate.

2D3 Source Lamp Power Supply (Refer to Figure 2D-2.)

The colorimeter lamp supply transforms a 12-volt rms a-c voltage into a regulated 7.2-V d-c output voltage. The power supply consists of a voltage regulator, printed circuit board, bridge rectifier, and input filter capacitor.

The a-c input to the module is 12 Volts at 50 or 60 Hz. Bridge rectifier CR1 converts the a-c input to 5 V dc. Capacitor C1 provides the input filtering and the storage capacity required to hold the d-c output constant when there is an a-c line dropout.

Voltage regulator VR1 is a positive 5-volt regulator capable of delivering 10 amps. A boost circuit consisting of resistors R1, R2, R3, R4 and trim pot R5 increases the regulator output from 5 V dc to 7.2 V dc.

Voltage regulator VR1 contains short circuit current-limiting and thermal-overload protection circuitry designed to shut off if the current or temperature are out of limits. To prolong lamp life, the output of the supply will drop to 5.1 V dc when the system is in the STANDBY mode.

In the STANDBY mode, a logic 1 command signal from the Stepper Motor Controller Board forward biases zener diode CR1, and switches on transistor Q1. Boost circuit resistors R1 and R2 are then bypassed, reducing the output voltage from 7.2 V dc to 5.1 V dc.

Figure 2D-2 FUNCTIONAL DIAGRAM OF 7.2-V D-C POWER SUPPLY

DATA ACQUISITION TIMING DIAGRAM

Figure 2DFO1 COLORIMETER CIRCUITS

2E FRONT PANEL ASSEMBLIES

This section describes the touch display module, indicator panel, printer, reaction tray preheater, and fluorescent lamp assemblies.

2E1 Touch Display Module (Refer to Figure 2E-1.)

The Fluke 1780A Infotouch Display Module replaces the TECHNICON RA-1000 system key pad for data entry and system control functions. Also, some of the prompts and messages formerly output by the thermal printer are now displayed on the 1780A CRT. At system start-up, the 1780A displays the diagnostic test sequence along with error messages.

2E1.1 Touch Display Communication

The RA-XT main CPU communicates bidirectionally with the Fluke 1780A Infotouch Display Module through RAM Disk Board USART U29. Address 0F8h selects U29 for a data transfer. Address 0F9h selects U29 for a status update or a control function. The -RD and -WR inputs to U29 determine direction of data flow (see Table 2-7). Data flow to and from the Fluke A1 PCB is through an RS-232-C interface.

Table 2-7 U29 DATA FLOW

ADDRESS	C/D	RD	WR	OPERATION
0F8h	0	0	1	U29 Data → Data Bus
	0	1	0	Data Bus → U29
0F9h	1	0	1	Status → Data Bus

2E1.1.1 Start-up Diagnostics

Because the 1780A display module is integral to start-up diagnostics and program download, it is the first subsystem to be checked following initialization. After allowing sufficient time for the 1780A self test, the RA-XT CPU sends character string **<ESC> [6 n** to the 1780A at 9600 baud. These characters represent a cursor position request. The CPU then waits 20 milliseconds during which time it expects to see **< ESC >** as the first character returned from the 1780A. If 20 milliseconds elapse with no response, the CPU again sends a cursor position request.

The CPU makes 80 attempts to communicate with the 1780A, each attempt lasting 20 milliseconds. If by the end of this period the 1780A has not responded, the program is aborted and the STANDBY, READY, and OPERATE lights cycle continuously on and off.

Failure by the 1780A to respond correctly can be caused by improperly set function and baud rate switches at the rear of the 1780A. Correct settings are as follows:

Switch S1

POSITION	SETTING	FUNCTION
1	Down	No Parity
2	Down	Odd/Even
3	Down	1 Stop Bit
4	Up	8 Data Bits
5	Down	Test Mode OFF
6	Down	Auto Line Feed OFF
7	Down	Auto Wraparound OFF

Switch S2

Set to position 7 (9600 Baud)

In addition, the 1780A power switch should be ON.

Figure 2E-1 TOUCH DISPLAY COMMUNICATION

2E1.1.2 Touch Screen Inputs

Scanning of the touch screen overlay for inputs is accomplished by column decoder U10, a 4-input BCD-to-decimal decoder whose output is active low. The A1 CPU (U28) outputs a column address for each of the overlay's ten columns. As each column in turn is brought low (scanned), multiplexer U39 monitors the six row output lines. Pressing a touch-sense key in an enabled column closes the row-column switch, and brings the row output low. U39 then signals CPU U28 that a selection has been made. The selected key number is output to the RAM Disk Board through UART U35.

2E1.1.3 Display Control

The RA-XT CPU stores ASCII character codes in RAM memory on the RAM Disk Board. These 8-bit codes are sent to the 1780A Infotouch Display via USART U29. The ASCII codes are interpreted by the 1780A CPU (U28) as addresses to its own RAM (U20).

U20 is a 2K RAM IC logically divided into 16 lines of 128 bytes each. The first 80 bytes of each line are reserved for ASCII character codes. Hence, 1280 characters can be stored. When selected, U20 forwards the character codes to CRT Controller U33 along data lines D0-D7.

CRT Controller U33 contains two character buffers. Each buffer can hold one row of 80 characters. While one buffer is being used to display the current row, the other buffer is loaded with the next row. The CRT Controller is responsible for providing the Character Generator PROM (U32) with the character codes, maintaining the character line count, and producing horizontal and vertical retrace signals and attribute data.

2E1.1.4 Character Generation

Characters displayed by the 1780A are composed of fourteen 8-bit lines. It is the task of the character generator PROM to output the line configuration of ones and zeros for each character, line by line. Character Generator U32 monitors character code lines CC0-CC6 from CRT Controller U33, and four line-count lines from "Row" Counter U6. The A11 input to U32 is tied to +5V dc. A 12-bit address is thus composed to access character lines from PROM.

The character generator PROM contains each of the fourteen 8-bit line configurations of ones and zeros for every character contained in RAM. Row Counter U6 is synchronized with a line counter internal to the CRT Controller. The line count is incremented with each horizontal retrace (HRTC) output pulse from the CRT Controller.

During a vertical retrace (VRTC), the line counter is disabled until the electron beam returns to its starting position at the top of the screen. The horizontal retrace frequency is approximately 15 kHz. The vertical retrace frequency is the same as the a-c power line frequency (50/60 Hz).

Character generator outputs are sent to Shift Register U8. The character line code bits shift out of U8 at the dot clock frequency of 12.77 MHz. Parallel load (LD) pulses to the shift register occur on every eighth dot clock pulse. LD is derived from the terminal count (TC) output of Presettable Counter U4.

Counter U4 is preset with a binary count of 1000 (decimal 8) so that seven dot clock pulses later, its terminal count is 1111 (decimal 15), and Shift Register U8 is loaded with the next 8-bit character line code from the character generator. The Qc output of Counter U4 is a square wave also one-eighth the dot clock frequency. This output is ANDed with Character Clock Enable (CCLKEN) to provide a clock signal (CCLK) to CRT Controller U33. CCLKEN is derived from the Horizontal Sync Logic circuitry, and is used to disable the clock input to U33 during a horizontal retrace. Timing relationships are shown in Figure 2E-2.

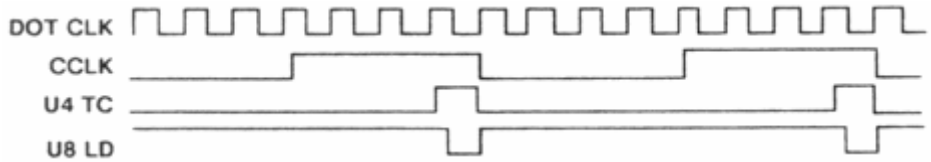


Figure 2E-2 CHARACTER LOAD AND SHIFT TIMING

2E2 Indicator Panel (Refer to Figure 2E-3 and Schematic 108-C809.)

The TECHNICON RA-XT system Indicator Panel contains the clock module, time/alarm set switches, and a PC board containing indicator lamps, drivers, and fan strobe one-shots. Signals arrive at the indicator panel from various parts of the system. Figure 2E-3 shows pin-to-pin connections.

2E2.1 Clock Module

The Indicator Panel Clock Module (P/N 679-6073-01) is a 28-pin integrated circuit containing the clock movement and LED display in a single package. A 28-pin flex cable connects a-c power and switch inputs to the module.

The Clock Transformer's (P/N 108-B846-01) 117-V a-c input is fused with the main system power line *before* the main circuit breaker. *When system power is shut off, the clock transformer continues to deliver 3.5 V ac and 7.5 V ac to the clock module.*

WARNING

To avoid electrical shock hazard, shut off system power and unplug the power cord before servicing the TECHNICON RA-XT system.

2E2.1.1 Programmable Inputs

Jumpers P2 and P3 provide for 50/60 Hz operation and 12/24 hour display modes. P2 connects pin 10 of the clock module to Vss (0 V ac) for 50 Hz. For 60 Hz operation, pin 10 is left open. P3 connects pin 11 of the clock module to Vss for a 24-hour format. If pin 11 is left open, the 12-hour format is selected. Jumper positions are tabulated in Figure 2E-3.

Figure 2E-3 INDICATOR PANEL

2E2.2 **Indicator Panel Lamps** (Refer to Schematic 108-C809 and Figure 2E-4.)

Each of the indicator panel lamps is powered by +5 V dc from TB3-2. A low logic level is required to turn the lamps on. The Indicator Panel PCB contains driver inverters to illuminate DS4-DS9. DS10 and DS-11 (TRAY PREHEATER) are illuminated by the Reaction Tray Preheater Assembly relay. Resistor R3 in series with DS10 and DS11 maintains the same illumination intensity as the other indicators. Resistors R4, R5, R6, and R7 allow a small trickle current to prolong lamp life.

The signals that arrive at Indicator Panel connector J3 - REACTION HEATER, REAGENT HEATER, and REACTION TRAY FAN - are connected in parallel with Alarm Control Board connector J2. The fan strobe circuitry on the Indicator Panel PCB is similar to that on the Alarm Control Board. Circuit operation is as follows: The reaction tray fan outputs a 20-ms square wave when it is rotating. The fan strobe signal is buffered and inverted before arriving at two one-shots. The first one-shot triggers on the rising edge of the strobe pulse. The second one-shot triggers on the falling edge of the strobe pulse. The positive output pulses from the one-shots, 19 ms in duration, are inverted and input to AND gate U3. Since one of the inputs to U3 will always be low while the fan is operating properly, the output of U3 is held low. This low output is then inverted by U4, and the REACTION TRAY FAN lamp remains off.

If the reaction tray fan fails, or operates too slowly, the output of AND gate U3 goes high, and the lamp is illuminated. An alarm signal is simultaneously sent to the CPU from the Alarm Control Board.

Figure 2E-4 RAM DISK BOARD INDICATOR CONTROL AND SWITCH MONITORING

2E2.3 **Operating Mode Lamps** (Refer to Figure 2E-4.)

STANDBY, READY, and OPERATE mode lamps on the indicator panel are illuminated when a low logic level is output to each lamp. These controlling signals originate at RAM Disk Board PIA U21 ports PC0, PC1, and PC2, respectively.

Address 0F6h from the CPU selects PIA U21 and enables output port C. The three low order data bits appearing on the U21 data bus at this time set the lamps ON or OFF. U17 is an inverting Darlington driver IC capable of sinking currents necessary for lamp illumination.

Following is a description of the operating modes.

- **Standby Mode** (Refer to Figure 2E-5.)

When the system is powered on, the STANDBY lamp illuminates, and power is applied to the colorimeter lamp, reagent preheater, reaction tray air bath, and the system electronics. A 30-minute counter begins to count down in order to ensure temperature stabilization of the preheater and air bath before entering the READY mode.

At the end of the 30-minute warm-up period, the READY lamp illuminates if the monitored temperatures are within limits. If either temperature is out of range at the end of the 30-minute period, the READY lamp remains unlit, and the CRT displays TEMP.

It is possible to operate the system before completing the 30-minute warm-up period. This is accomplished by selecting BYPASS WARMUP from the Start Up screen.

- **Ready Mode**

The system enters the READY state 30 minutes after being powered on if the preheater and air bath temperatures are within range. The system remains in this mode until a work list is entered and the OPERATE key is pressed. If a hardware error occurs during this state, the system will automatically revert to the STANDBY mode, and will display the error on the CRT.

- **Operate Mode**

In the OPERATE mode, test data are processed and reported. This mode is active from the beginning of sampling to the reporting of the last test on the work list.

Typing the number of the work list previously entered, and pressing the OPERATE key illuminates the OPERATE lamp and initiates sampling.

If the temperature is out of range, or there is a hardware problem during the OPERATE mode, the hardware or temperature error flashes on the CRT, and the system automatically reverts to the STANDBY mode.

2E3 **ALARM RESET and PAPER FEED Switches** (Refer to Figure 2E-4.)

ALARM RESET and PAPER FEED push-button switches are monitored through RAM Disk Board PIA U21 ports PB0 and PB1, respectively. Pressing the push-button switches inputs low logic levels to monostable vibrators (one shots) U18. With each low-to-high transition of the 2-MHz clock input to U18 (pins 2 and 10) a 100-nanosecond positive pulse is issued from the vibrators to PIA U21. The CPU reads these pulses by issuing address 0F5h, which enables U21 input port B.

Figure 2E-5 MODE CHANGE LOGIC

2E4 Printer

The printer is a forty-column thermal plotter. It is a dot matrix printer with graphics capabilities, and can print any character or symbol that can be formed within the five by seven dot format. Each character is five dots wide by seven dots high.

Each set of two characters is 14 dots wide by 10 dots high. There are two blank dots between the two characters, one dot flanking each character, and three rows of dots between lines of print - altogether a 140-dot matrix (see Figure 2E-6).

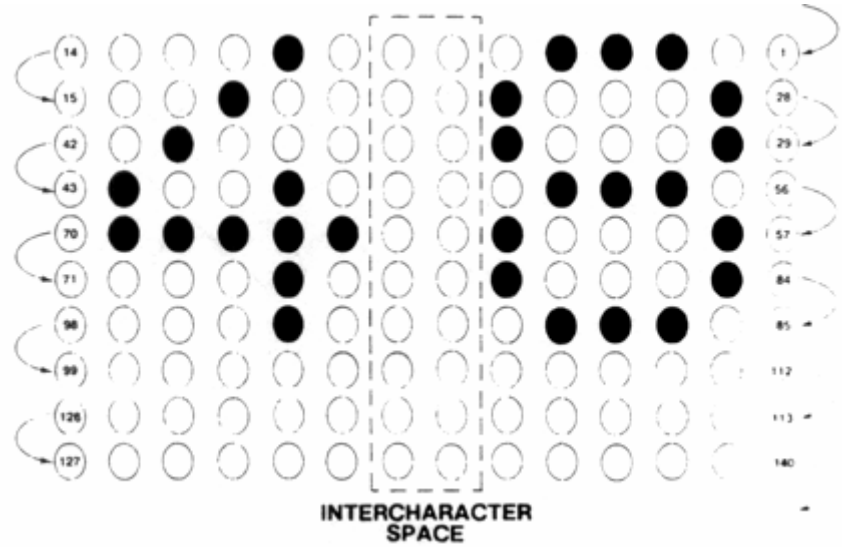


Figure 2E-6 PRINTER DOT MATRIX

Voltages to the thermal elements are individually controlled by the Printer Controller Board (P/N 527-5098-03). The Printer Controller Board receives +24 V dc from PS2 (1TB5) and +5 V dc from PS1 (1TB8).

There are no adjustments required for the thermal printer. To check print quality, select exerciser test THERMAL PRINTER. This test produces a printout of the full character set (see Figure 2E-7). If the print quality is poor or nonexistent, verify that the paper is properly loaded (only one side of the paper is thermosensitive). Figure 2E-8 shows proper paper loading.

NOTE

After loading paper the platen release lever must be returned to the engaged position. Failure to reset the platen release lever inhibits data transmission to the printer.

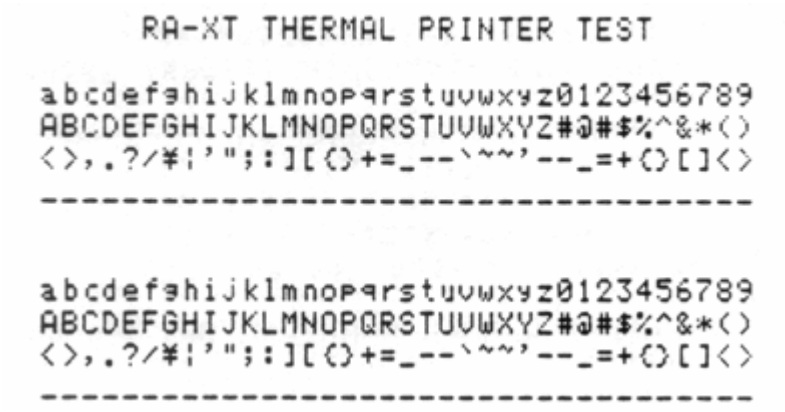


Figure 2E-7 THERMAL PRINTER EXECISER TEST PRINTOUT

Figure 2E-8 THERMAL PRINTER PAPER LOADING

If the printer still does not print after checking the paper and the setting of the platen release lever, execute the printer self-test to determine if there is a data transmission problem. The printer self-test is executed by first shutting OFF power to the system. Connect pin 29 (FEED) of connector CN1 to pin 30 (GND). Apply power to the system. The printer will print the test pattern shown in Figure 2E-9. Shut OFF system power to terminate the test.

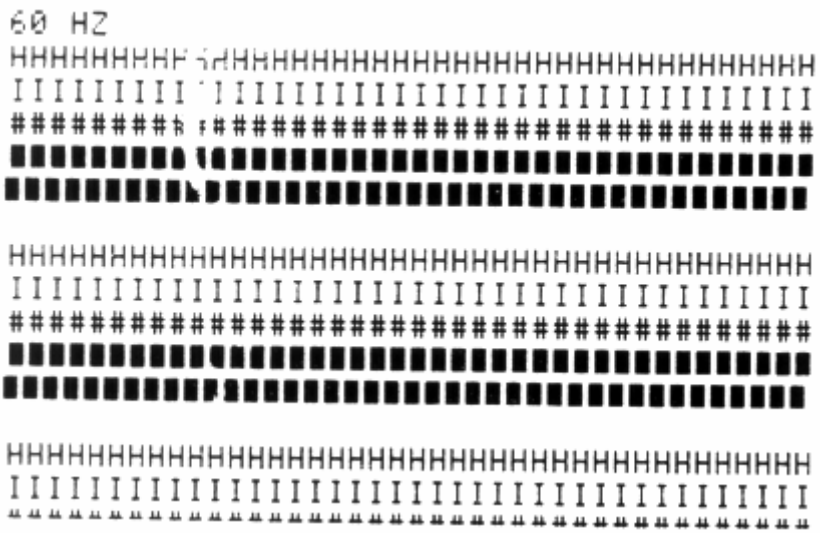


Figure 2E-9 THERMAL PRINTER SELF-TEST PRINTOUT

2E4.1 Printer Interface (Refer to Figure 2E-10.)

Figure 2E-10 provides a functional description of how the printer interfaces with the Stepper Motor Controller Board.

The main computer addresses PROM U28 to select universal peripheral interface (UPI) U32. This IC communicates with the 8085 CPU along a data bus. Transceiver U29 on the Stepper Motor Controller Board controls direction of data flow.

UPI U32 communicates with the Printer Controller Board, resident in the printer assembly, along data lines D1-D8 and a strobe line. Scrambler Board 108-B803-01 is used to reroute data and control lines since connector pin configurations on the Stepper Motor Controller Board and the Printer Controller Board do not match. The Scrambler Board also contains pull-up resistors.

Figure 2E-10 PRINTER INTERFACE

2E5 Reaction Tray Preheater (Refer to Figure 2E-11.)

The TECHNICON RA-XT system contains an oven located to the left of the indicator panel for preheating reaction trays to 30癈 or 37癈. The heater elements operate on, 117 V ac from Temperature Controller #1.

The Reaction Tray Preheater switch assembly contains a relay, which, when energized closes a path to ground to illuminate the TRAY PREHEATER lamp.

2E5.1 Temperature Control

Under normal operation, the reaction tray preheater elements switch on and off in conjunction with the reaction enclosure heater elements. Switching for both assemblies is controlled by the reaction module heater control circuit.

Should the Temperature Controller One TRIAC fail, the Reaction Tray Preheater Assembly thermostat (P/N 694-0104-03) will open when the preheater temperature exceeds 55癈. The thermostat closes again when the temperature falls to between 48.3癈 and 52.8癈.

Figure 2E-11 REACTION TRAY PREHEATER INTERCONNECT DIAGRAM

2E6 Fluorescent Lamp

The TECHNICON RA-XT system contains a fluorescent lamp fixture situated above the PD pump assembly. The starter/ballast assembly for the fluorescent lamp is located in the rear of the system near the main circuit breaker.

2E6.1 Circuit Operation (Refer to Schematic 108-C807, Sheet 2 of 3.)

When power is initially applied, the starter acts like a closed switch supplying 117 V ac to the lamp. Once the gas within the lamp is ionized, its resistance approaches zero, and it begins to conduct. The starter capacitor discharges and becomes an open switch, no longer supplying 117 V ac to the lamp terminals.

The ballast functions as a high voltage coil to ionize the gas on start-up. The lamp used is rated at 4.0 Watts with a life expectancy of about 4,000 hours.

2F TEMPERATURE CONTROLLERS ONE AND TWO (Refer to Figure 2F-1.)

The RA-XT system contains two temperature controllers. Controller One maintains the temperature of the air circulating in the reaction module enclosure at 30癈 or 37癈, and simultaneously powers the heater elements in the Reaction Tray Preheater Assembly. Controller Two maintains the reagent preheater at a temperature that will heat the reagent to the assay temperature of 30癈 or 37癈.

The temperature controller assembly consists of controller boards one and two, and an alarm board. Controller One is positioned above Controller Two on the mounting plate. Potentiometer R1, switch S1, lamp DS1, and plug in triac TC1 are part of the Controller One assembly. Potentiometer R2, ambient thermistor RT1, switch S1, lamp DS2, plug in triac TC2, and potentiometers R3 and R4, mounted on a separate printed circuit board, are part of the Controller Two assembly.

2F1 Reaction Module Heater Control Circuit (Refer to Figures 2F-1, 2F-2, and 2F-3.)

Controller One is supplied an operating voltage of 115V ac. Lamp DS1 indicates when the air circulating in the reaction module enclosure is at the proper temperature by going from constantly on, to blinking on and off. The temperature level is selected by setting switch S1 on the controller assembly to either the 30癈 or 37癈 position. In the 30癈 position, switch S1 removes potentiometer R1 from the thermistor circuit. Potentiometer R26 is set to the reference voltage. In the 37癈 position, switch S1 is set so that potentiometer R1 is in series with the thermistor. The Reaction Tray Preheater is a resistive load in parallel with the Reaction Module heater when switched on.

The resistance of the thermistor in the reaction module enclosure decreases as the temperature increases. The resulting change in voltage is monitored by the controller so the temperature can be kept within the limits set by R26 and R1 for 30癈, or R26 for 37癈. If the controller fails to maintain the proper temperature, an alarm circuit will be actuated.

2F2 Reagent Preheater Control Circuit (Refer to Figures 2F-1, 2F-4, and 2F-5.)

Controller Two is supplied an operating voltage of 24V ac. Lamp DS2 indicates when the reagent preheater is at the proper temperature by blinking on and off. The temperature level is selected by switch S1. The temperature of the heater in the reagent probe arm is set higher than the 30癈 or 37癈 assay temperature. The higher temperature is required to heat the reagent, which is at room temperature, to about 0.5癈 above the selected assay temperature. If the ambient temperature should exceed a preset limit, the reagent preheater set point temperature is adjusted to compensate. The ambient temperature thermistor is used as the sensor to detect a temperature change.

In the 30癈 position, switch S1 removes potentiometer R2 from the circuit and places potentiometer R3 in parallel with the ambient thermistor. Potentiometer R26 on Controller Two is set to the reference voltage.

In the 37癈 position, switch S1 places potentiometer R4 in parallel with the ambient thermistor, and connects potentiometer R2 into the circuit. As in the Controller One circuit, the resistance of the thermistor in the reagent arm decreases as the temperature increases. The resulting change in voltage is monitored by Controller Two to keep the preheater at the proper temperature. If the controller fails to maintain the proper temperature, the alarm circuit is actuated to alert the system microprocessor.

Figure 2F-1 TEMPERATURE CONTROLLER CIRCUITS

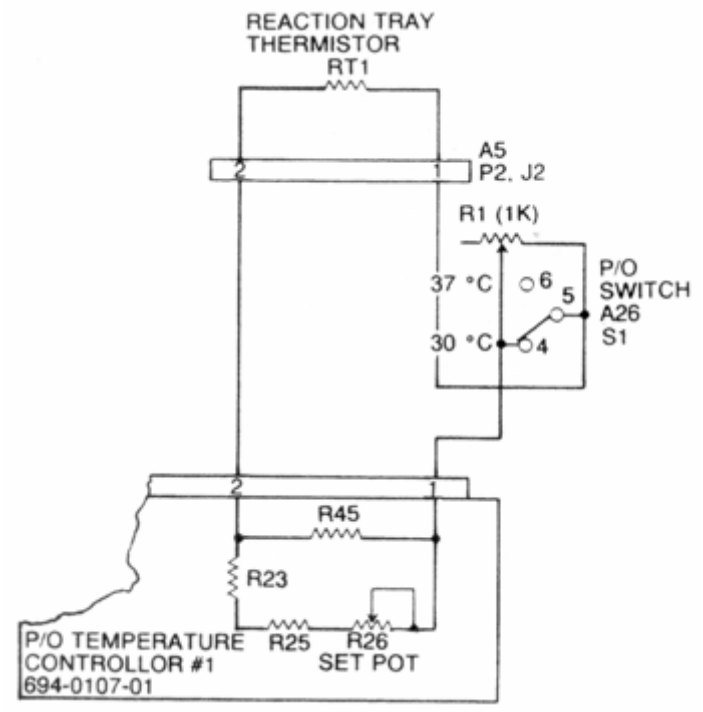


Figure 2F-2 REACTION MODULE ENCLOSURE 30°C THERMISTOR SENSING CIRCUIT

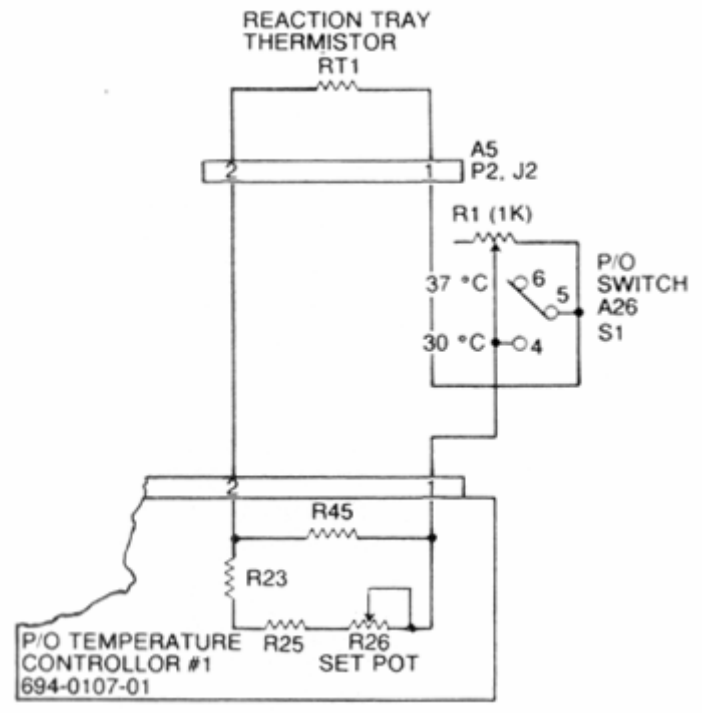


Figure 2F-3 REACTION MODULE ENCLOSURE 37°C THERMISTOR SENSING CIRCUIT

Figure 2F-4 REAGENT PROBE ARM PREHEATER 30°C THERMOCOUPLE SENSING CIRCUIT

Figure 2F-5 REAGENT PROBE ARM PREHEATER 37°C THERMOCOUPLE SENSING CIRCUIT

2F3 Reaction Module Heater and Reagent Preheater Elements

The heating elements in the reaction tray module and the reagent probe arm are protected by a thermostat in series with each heater. If the temperatures in the reaction module or the reagent probe exceed the heat rating of the thermostats, the contacts on the thermostats, which are normally closed, will open and interrupt the supply voltage to the heater. A fan in the reaction module circulates the air through the heating element in the reaction chamber.

2F4 Controller Boards One and Two Circuits

The a-c voltage supplied to the respective controllers is rectified on the controller board for use by the time proportioning zero-volt switching circuit, and the alarm control circuit. The time proportioning circuit makes use of a TRIAC on-off controller with an IC zero-voltage switch. The IC is a combination zero-voltage sensor and trigger circuit. The triac is turned on near the zero crossing by a pulse from the IC to the trigger gate whenever the voltage across the thermistor exceeds the reference voltage.

If the temperature for the reaction module or the reagent probe arm goes above or below the preset alarm limits, it will cause the alarm circuit to turn on. The alarm output signal goes from 3.2 volts when off, to 0.8 volts when on.

2F5 Alarm Control Board (Refer to Figure 2F-1.)

The Alarm Control Board monitors the alarm outputs from Temperature Controllers One and Two, and the reaction module fan strobe output. If one or both temperature controllers output an alarm signal, or the fan slows down or stops, the circuits on the Alarm Control Board will cause the respective LED to illuminate, and simultaneously will issue a signal to alert the 礙 of the condition.

The fan outputs a 20-ms square wave strobe signal during normal operation. The strobe signal enters the Alarm Control Board at pin 3 of J2 and is directed to U3 pin 3, and U3 pin 5. At U3-3, the signal is inverted and the negative edge triggers one shot U1 to produce an output pulse width of 19 ms from U1-6. One shot U1-12 is triggered by the positive edge, and produces an output pulse width of 19 ms. The outputs from one shot U1-6 and U1-10 are inverted by U3-2 and U3-12, and produce a logic 1 at the output of NAND gate U4-3 under normal operation.

When the fan is not operating, or operates too slowly, neither one shot is active and the output of U4-3 is a logic 0. The logic 0 turns on LED DS3 and change and changes the output of gate U2-8 from logic 0 to a logic 1.

The alarm signals for Temperature Controllers One and Two enter the board at pins 1 and 2 respectively. The alarm board circuits for both controllers are identical. When a logic 0 Temperature Controller One alarm signal is issued to pin 1, it is inverted to a logic 1 by U3, which changes the output of gate U4-8 to a logic 0. The logic 0 turns on LED DS1 and makes the output of gate U2-8 go to a logic 1. The Alarm Control Board makes provision for five spare alarm circuits.

The signals at pins 1, 2, and 3 are tapped off and sent to the indicator panel where they are electrically conditioned to operate the indicator lamps (see Figure 2E-3).

2G CPU/MEMORY/DISK CONTROLLER BOARD (Refer to Figure 2GFO1.)

The CPU/Memory/Disk Controller Board is the system controller for the RA-XT system. It includes the following:

- CPU - An 8085 microprocessor, an 8257 DMA controller, and supporting circuitry make up the 8-bit central processing unit.
- Memory - 64k of dynamic RAM supported by an 8202 dynamic RAM controller IC. There is also 4k of PROM for the start-up program.
- Disk Controller - An 8272 (or NEC 765) integrated circuit and support circuitry can control 1 to 4 drives. The drives can be 5 1/4 in. or 8 in., single or double density.
- Serial I/O - Two serial I/O channels for use with a CRT and printer (for future use).

The board provides the standard multibus signals for an 8-bit data bus and a 16-bit address bus. Three additional address lines are produced on the CPU/Memory/Disk Controller Board, which allow memory space greater than 64k if it becomes necessary in the future.

Figure 2GF01 is a block diagram of the CPU/Memory/Disk Controller Board. The CPU circuitry includes the 8085 microprocessor, the DMA control circuit, the ready controller, the address decoder, the 8155 I/O device, the status decoder, the bus controller, and the arithmetic processor.

The buses on the CPU/Memory/Disk Controller Board are controlled either by the 8085 microprocessor or by the DMA control circuit. DMA is the abbreviation for Direct Memory Access, and refers to data transfers that occur without involvement of the 8085. During a normal (non-DMA) data transfer, the 8085 inputs a word from the source, and outputs the word to the destination. During a DMA transfer the 8085 relinquishes control of the buses, and the DMA control circuit transfers a block of data from the source to the destination at high speed. In the RA-XT system, DMA transfers are from disk to memory or from memory to disk.

Because the 8085 has a multiplexed data/address bus, the DMA control circuit latches the low order data byte even when the 8085 is controlling the buses.

When DMA transfers are not occurring, the 8085 is the controller. When the system is reset, the 8085 begins executing the start-up program located in PROM. After the start-up tests are completed, the operating program (or exerciser) is loaded into RAM Disk Board memory, and the 8085 then executes instructions out of memory until another reset (or power on) occurs.

The address decoder produces the required chip select signals by decoding the high address byte. Three additional address control inputs are sent by the 8085, via the 8155, to the address decoder. These signals - MEMORY CONTROL 1, MEMORY CONTROL 2, and MEMORY CONTROL 3 - are used in decoding EXTERNAL MEMORY SELECT, PCS (protected chip select), PROM ENABLE, and the three extra address bits (not shown in Figure).

The 8155 is a parallel I/O device similar to the 8255. In addition, it contains a 256-byte RAM and a timer. The 8155 is directly compatible with the 8085, which means that it accepts the multiplexed address/data bus and the ALE (address latch enable) signal.

Three 8155 outputs are used for memory control as described above. Eight of the I/O lines are inputs from the configuration DIP switch located on the CPU/Memory/Disk Controller Board. The function of each switch is listed in the block diagram.

One 8155 I/O line is the UNIT ENABLE input. Via the UNIT ENABLE signal, the 8085 has the capability of relinquishing control of the disk and the card cage buses. In the RA-XT system, UNIT ENABLE is always high.

The four remaining I/O lines are dedicated to the disk. The DISK INTERRUPT REQUEST input allows the 8085 to monitor the disk controller interrupt request. The DISK CLOCK CONTROL output selects one of two disk write clock frequencies (for five-inch or eight-inch drives). The MOTOR ON signal is used to turn the disk motor OFF when disk reading or writing is not required.

The bus controller interfaces the card address and data lines to the backplane address and data lines. Should UNIT ENABLE become inactive, the card cage address and data lines would be placed in a high impedence state.

The status decoder produces the on card status signals (-MR, -MW, -IR, -IW) and the card cage status signals (MRDC, MWTC, IORC, IOWC). Should UNIT ENABLE become inactive, the status lines would be placed in a high impedence state. Otherwise, the 8085 controls the lines for non-DMA transfers, or the DMA control circuit controls the lines for DMA transfers.

The ready controller creates 8085 wait states by putting a low on the READY line. This allows synchronization with the XACK signal returned by other card cage boards, as well as allowing wait states to be introduced for slow on-card devices.

The CPU board memory includes four circuits: the memory bank, the memory decoder, the memory latch, and the 8202 dynamic RAM controller. To conserve pins on the RAM ICs, the address is sent to the RAM in two groups, called the row address and the column address. The dynamic RAM controller provides address lines A0-A6, and the RAS and CAS (row address strobe and column address strobe) signals. The A7 address line comes from the memory decoder. Data read from the memory is stored in the memory latch. The tri-state outputs of this latch drive the data bus. Data is written into the memory directly from the data bus.

2G1 RAM Disk Board Memory (Refer to Schematic 108-C804.)

The RAM Disk Board (P/N 108-B804-01) provides 512K bytes of additional memory capacity. The name "RAM Disk" is used to distinguish it from "floppy" disk and "hard" disk. Data can be retrieved from the RAM Disk Board at a much faster rate than from the RA-XT floppy disk drive. When the TECHNICON RA-XT system is powered up or reset, the entire operating program is downloaded to the RAM Disk Board following start-up diagnostics. During a write operation, data is transferred simultaneously to RAM disk and to floppy disk.

RAM Disk memory is comprised of two banks of 256k dynamic RAM ICs, a RAM controller, five up-counters, and logic circuitry for generating a refresh clock and address strobes. Memory locations are addressed through the data bus when inverter buffer U56 is enabled by -RAM from U54, a programmable array logic (PAL) device. The data output of buffer U56 makes up a starting address that is then latched by five up counters. Each of the five up counters monitors four lines of the data bus. Latching of the data bits is controlled by the -LOW, -MED, and -HI outputs from U54. A low logic level to the parallel load (-LD) input of each counter latches the four bits and places them on the cross-hatched address bus. Counters U33 and U34 latch the low order eight bits; U32 and U30 latch the middle bits; and U31 latches the high order bits.

A composite 18-bit address, plus two bits, is presented to RAM Controller U27. Half of the 18-bit address represents a row address; the other nine bits represent the column address. Address bit A18 is used to select Row Address Strobes -RAS0 and -RAS1. A low logic level on A18 actuates -RAS0; a high logic level actuates -RAS1. -RAS0 selects the upper bank of RAM: -RAS1 selects the lower bank. Address bit A19 selects -RAS2 and -RAS3, and is not used.

The two banks of RAM are composed of 1x256k dynamic RAM ICs. There are eight of these 41256 DRAMs in each bank. Each chip stores one bit of an 8-bit word in each memory cell. Each bank of RAM can store 256k 8-bit words.

During a read operation, the beginning memory address is latched into Counters U30-U34, and placed on the address bus. The ripple clock outputs (-RCO) of the counters are connected to the device enable inputs (-G) of adjacent counters. With each column address strobe (-CASALL), the counters increment and output the next consecutive memory address.

Each RAM IC of a selected bank outputs one bit of data at a time onto a dedicated line of the RAM data bus. The RAM data bus lines are connected to the IN and OUT pins of each RAM chip. Data input and output operations are controlled by the Write Enable (WE) input of each RAM chip. Memory refresh occurs every 500 nanoseconds, except when a read or write operation is in progress. A 9-bit refresh counter internal to the RAM Controller is incremented with each row refreshed, thereby supplying the next refresh address.

2G2 DMA Control (Refer to Figure 2G-1.)

The DMA control circuit manages control of the address bus. Most of the work is performed by the 8257 DMA controller. The 8257 is capable of processing DMA requests from four sources. In the RA-XT, there are only two DMA channels in use, which transfer data between floppy disk and CPU memory, or between floppy disk and RAM disk memory.

To understand the address bus control scheme, the bus structure of the 8085 and the 8257 must be known.

The 8085 outputs the high order address byte onto its A8-A15 lines. The low order byte is output onto the multiplexed address/data bus AD0-AD7. When the 8085 is controlling the address bus, it is necessary to latch the low order address byte from AD0-AD7 on the occurrence of ALE. This is the purpose of the low byte address latch.

In the 8257, things are backwards! That is, the low order address byte is output directly onto the 8257 A0-A7 output lines. The high order address byte is output onto the AD0-AD7 lines, and must be latched on the occurrence of the ADDRESS STROBE. This is the purpose of the high byte address latch.

Notice that the low-byte latch receives AEN at the OE input, while the high byte latch receives AEN at the OE input. Thus the low byte latch is enabled when the 8085 is in control (AEN low, AEN high). The high-byte latch is enabled when the 8257 is in control (AEN high, AEN low). Since the latches have tri-state outputs, the unused latch is effectively out of the circuit.

As noted above, the AEN output of the 8257 specifies the controlling device. When a DMA transfer occurs, a series of events occurs involving the 8085, the 8257, and the 8272 (disk controller).

Figure 2G-1 DMA CONTROL

Suppose a read from disk into memory is desired. More specifically, suppose we wanted to read track 00 sector 1 and store it in memory at address 4000h. The following events would occur:

1. The 8085 would, via an I/O write, inform the 8257 that a DMA operation is upcoming on channel 0. The 8085 specifies the number of bytes (256).
2. The 8085 instructs the 8272 (disk controller), via an I/O write, to read track 0 sector 1.
3. The 8272 requests a DMA transfer by actuating the DRQ line.
4. The 8257 requests that the 8085 put itself in the hold state and relinquish control of the buses. This occurs when the 8257 actuates its HRQ output.
5. The 8085 puts itself in the hold state and actuates its HLDA output.
6. The 8257 instructs the disk controller to proceed by actuating its DACK output.
7. 255 bytes are transferred.
8. During transfer of the 256th byte, the 8257 actuates the TC line, informing the disk controller that the last byte is being processed.
9. After the 256th byte is transferred, and the disk controller deactuates DRQ, the 8257 deactuates DACK.
10. The 8257 deactuates HOLD.
11. The 8085 deactuates HLDA and regains control of the buses.

Note that the DMA controller outputs four status signals: DMA IR, DMA IW, DMA MR, and DMA MW. These are multiplexed onto the status lines during DMA operations (in the status decoder circuit).

2G3 Ready Controller (Refer to Figure 2G-2.)

The ready controller circuit produces the microprocessor READY input. When READY goes low, the 嚽 enters a wait state. During the wait state, the 嚽 address and data lines are frozen. (Contrast this with the hold state, where the 8085 relinquishes control of the bus to the 8257.) The wait state (or states) may be required by slow-responding peripherals both on and off the CPU/memory/disk controller board.

Four conditions can cause the ready line to go low. Each of these conditions provides and active low input to OR gate U59-8.

The first input to OR gate U59-8 is the ARITH WAIT signal from the 9511 arithmetic processor. An active ARITH WAIT indicates that a 9511 calculation is in progress.

RAM WAIT, the second input to U59-8, disables READY when RAM SEL is active and SACK is inactive. RAM SEL is an 8202 RAM controller input from PROM that signals the beginning of a read or write operation involving the 64k CPU board resident dynamic RAM. READY remains low until the 8202 SACK (System Acknowledge) output goes low, indicating completion of the memory transaction.

The third input to OR gate U59-8 is from NAND gate U44-8. The lower input to U44-8 is high when EXTERNAL SELECT and either RD or WR is active. The upper input to U44-8 remains high until EXT ACK from the RAM Disk board goes low. A minimum wait period is forced by the QD output of Shift Register U34.

The fourth input to OR gate U59-8 comes from flip-flop U67-8. The Q output of U67-8 goes low with each ALE strobe, which in turn causes U67-5 to go high. The high U67-5 output is NANDed with an active RD or WR, or with AEIN, to reset U67-8.

Figure 2G-2 READY CONTROLLER

2G4 Bus Controller (Refer to Figure 2G-3.)

The bus controller circuit interfaces the on-card buses to the backplane buses. Bi-directional bus driver U65 interfaces the DAT0-DAT7 lines to the D0-D7 bus. The bus driver is enabled so long as UNIT ENABLE is active, except during the ALE pulse. The direction is derived from the RD and EXTERNAL SELECT inputs to NAND gate U17-3, OR gate U17-6, and flip-flop U16-5.

Figure 2G-3 BUS DECODER

The A0-A15 lines are transferred onto the AD0-AD9 and ADA-ADF lines by drivers U63 and U64. The drivers are enabled so long as UNIT ENABLE is active.

2G5 Status Decoder (Refer to Figure 2G-4.)

The status decoder circuit decodes the on-card and backplane status signals. Tri-state driver U60 gates MR, MW, IR, and IW onto the backplane status signals MRDC, MWTC, IORC, IOWC. When HLDA is actuated, the MRDC, MWTC, IORC, and IOWC lines are placed in a high impedance state, allowing some other board to transmit on those lines.

The MR, MW, IR, and IW signals are controlled by the 8085 during non-DMA data transfers, and by the 8257 during DMA transfers. When the 8085 is in control, multiplexer U31 is used to decode the 8085 RD, WR, and I/M outputs.

Figure 2G-4 STATUS DECODER

Figure 2G-5 ADDRESS DECODER

2G6 Address Decoder (Refer to Figure 2G-5.)

The address decoder produces the chip select signals required for the various I/O and memory data transfers. The I/O chip selects are decoded from address lines A8-A15 by PROM U-45 and decoder U46.

The memory chip select signals are decoded by PROM U32, with gate U59-6. In addition to address lines A8-A15, U32 also receives MEMORY CONTROL 1, MEMORY CONTROL 2, and MEMORY CONTROL 3 from the 8155.

The EXTERNAL SELECT signal is produced by gate U68-6 which ORs the I/O external signal with the memory external signal. The chip select for the 8155 is produced by ORing the I/O 8155 select with the memory 8155 select. This is necessary because the 8155 is both a memory (256 bytes) and an I/O device.

2G7 Memory Decoder (Refer to Figure 2G-6.)

The memory decoder produces memory address line A7, the column address strobe (CAS), and two memory timing signals, MR•RAM SEL and RD/S1. A7 is selected from A14 or A15. The CAS follows the CAS line from the 8202.

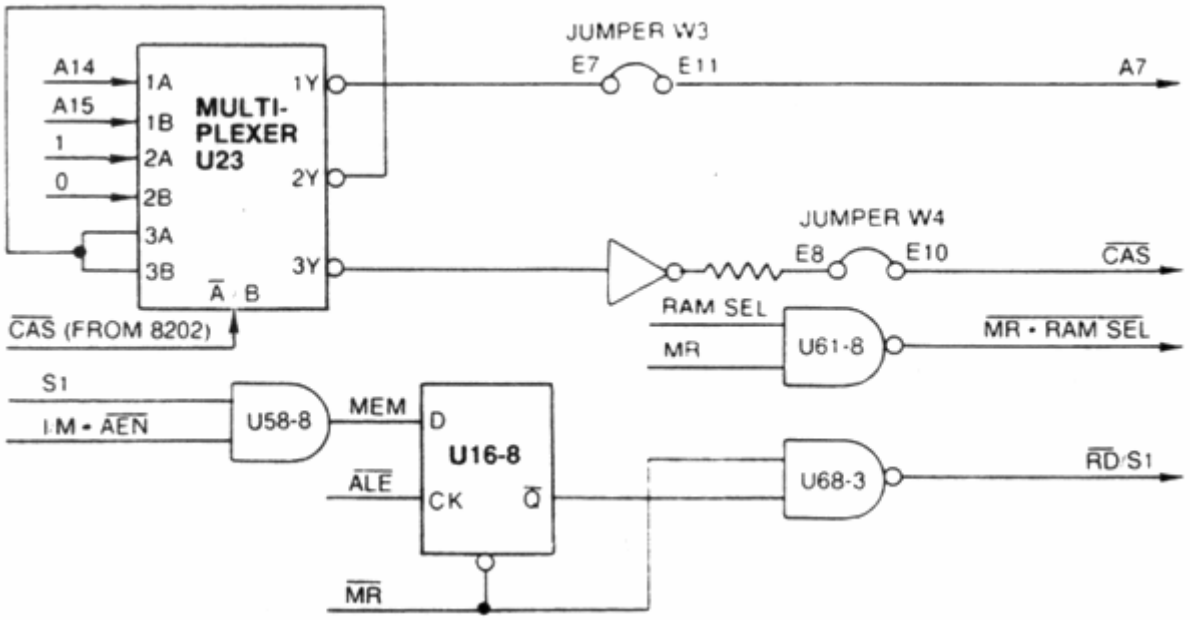


Figure 2G-6 MEMORY DECODER

2G8 Serial I/O (Refer to Figure 2G-7.)

Two RS-232 I/O ports are implemented using 8251A USARTs U19 and U20. Each USART receives a clock which originates at the 8253 interval timer; thus, the baud rate for each channel is independently programmable via the software.

Figure 2G-7 SERIAL I/O

2G9 Disk Controller (Refer to Figure 2G-8.)

The disk controller consists of:

- Disk Controller IC U42
- Decoding/encoding circuits for the multiplexed U42 lines.
- Data separation circuitry
- Double density write circuitry

2G9.1 Disk Controller IC

The disk controller IC produces signals for controlling up to four 5 1/4; in. or 8 in. floppy disk drives. All the outputs are ANDed with UNIT ENABLE, so that the capability exists for shared disk control.

The HDL output is used directly as HEAD LOAD. The HD output is used directly as SIDE SELECT. The RDY and IDX inputs receive, through buffers, the drive READY and INDEX signals.

Figure 2G-8 DISK CONTROL CIRCUITRY

Four U42 lines are multiplexed. They serve different functions during the seek and R/W modes. During R/W mode, the signals mean low current (LCT), fault reset (FR), fault (F), and write protect (WP). During seek mode, the signals mean direction (DIR), STEP, track 00 (TR), and two sided (TS). The U42 RW/SEEK output specifies the current mode.

U42 outputs two drive select signals, DS0 and DS1. These signals are decoded to select one of four drives.

The RDD and RDW lines are used to control and communicate with the data separation circuit. The WR DATA and WE signals communicate with the double density write circuits (U25, U28, and U29).

2G9.2 Decoding/Encoding Circuits for the Multiplexed Lines

Decoding and encoding of the multiplexed U42 lines is accomplished by the two sections of tri-state inverting buffers U13. During R/W mode operations, the upper section of U13 is enabled by the low -RW/SEEK line. LCT/DIR is transferred to LOW CURRENT, FR/STEP is transferred to FAULT RESET, FAULT is transferred to F/TR, and WRITE PROTECT is transferred to WP/TS.

During seek mode operation, the lower section of U13 is enabled by the low RW/-SEEK signal. LCT/DIR is transferred to DIRECTION, FR/STEP is transferred to STEP, TRACK 00 is transferred to F/TR, and TWO SIDED is transferred to WP/TS.

2G9.3 Data Separation Circuits

Data arrive from the disk in serial format with interleaved clock and data bits. The 9216B data separator IC (U26B) determines which pulses are clock pulses and which are data pulses. The disk controller IC is provided with read data (RDD) and read data window (RDW) inputs.

2G9.4 Double Density Write Circuitry

For double density writes, the precompensation circuitry (U25, U28, and U29) is required. Jumper W11 connects the C input of multiplexer U28 to + 5 V dc, removing the LOW CURRENT signal from the circuit. LOW CURRENT was formerly used to select single/double density operation.

2G10 Jumper Settings

The part number of the CPU/Memory/Disk Controller Board used in the TECHNICON RA-XT system is P/N 108-B148-04. Table 2-8 is a listing of the jumper settings to be used with this board.

Table 2-8 CPU BOARD JUMPER SETTINGS

JUMPER	SETTING
W1	E1 TO E2
W2	E5 TO E6
W3	E7 TO E11
W4	E8 TO E10
W5	E14 TO E15
W6	E16 TO E18
W7	E19 TO E20
W8	E23 TO E24
W9	E25 TO E26
W10	E28 TO E29
W11	E36 TO E37
W12	E43 TO E44
W13	E31 TO E32

Figure 2GFO1 CPU/MEMORY/DISK CONTROLLER BLOCK DIAGRAM

2H US, IDee, AND ISE INTERFACE

LIS, IDee, and ISE interface circuits are contained on the serial I/O printed circuit board (refer to Figure 2I-1). Three 8251A programmable communication interface devices (U8, U9, and U10) are used to transmit and receive data. An 8253 programmable counter (U11) is used as a baud rate generator to provide clock inputs to the three interface chips.

LIS interface device U8 has a driver IC (U1) to convert TTL levels to EIA RS-232 standard voltage levels. It also has a receiver IC (U2) to convert RS-232 to TTL levels. Conversion to TTY output is provided through 20-milliamp loop driver Q1. The IDee interface device (U9) and the ISE interface device (U10) also have driver and receiver level converters. The baud rate is software selectable from 9600 or 4800 down to 75 for RS-232 purposes.

2H1 8251A Interface Device (Refer to Figure 2H-2 and Schematic 108-C198.)

Interface devices U8, U9, and U10 are configured to operate in the asynchronous mode. The devices perform the following operations:

1. Convert output data from parallel to serial form; and, convert input data from serial to parallel form.
2. As transmitters they add start and stop bits, generate parity, and clock data out at the required baud rate. As receivers they recognize and delete start and stop bits, check parity, and clock data in at the required rate.
3. Provide indicators that signal whether they have received data, or are ready to accept data for transmission. The indicators may signify also errors in the received data.

A set of control words is sent by the 嚆 to initialize each 8251A IC to support the desired communication format. The control words are divided into two formats: mode instruction and command instruction.

The mode instruction format defines the general operational characteristics of the 8251A, and must be preceded by a reset operation (internal or external). The format consists of the baud rate, character length, parity enable, odd/even parity, and the number of stop bits. After the mode instruction has been entered into the 8251A, the command instruction follows.

The command instruction defines a status word that is used to control the actual operation of the 8251A. Functions such as enable transmit/receive, error reset, and modem control are provided by the command instruction. A reset command returns the 8251A to the mode instruction format.

The status of a data transfer can be monitored by the 嚆 for any evidence of an error. The status format includes: parity error, overrun error, or frame error as shown in Figure 2H-3.

Figure 2H-1 LIS, IDEE, ISE INTERCONNECT DIAGRAM

Figure 2H-2 SERIAL I/O BOARD

Figure 2H-3 STATUS READ FORMAT

2H1.1 Asynchronous Transmission (Refer to Figure 2H-4.)

Prior to transmitting data, the 磼 actuates the TRANSMIT ENABLE (TxEN) bit in the command instruction format, and receives a clear to send (CTS) signal. Whenever a data character is sent by the 磼, the 8251A automatically adds a start bit, followed by the data bits and the programmed number of stop bits to each character. The parity bit is inserted prior to the stop bits as defined by the mode instruction. Serial data is then shifted on the falling edge of TxD at a rate equal to 1/16 or 1/64 TxC (transmitter clock). The transmitter clock controls the rate at which the character is transmitted. In asynchronous transmission the baud rate is a fraction of the actual TxC frequency. After transmission TxD returns to the marking state (high).

2H1.2 Asynchronous Reception (Refer to Figure 2H-4.)

The RxD line is normally high. A falling edge on this line triggers the beginning of a start bit. The validity of this bit is verified at its nominal center by the internal bit counter. Data and parity bits appear at the RxD input on the rising edge of RxC (receiver clock). The receiver clock controls the rate at which the character is received. In asynchronous mode the baud rate is a fraction of the actual RxC frequency. A portion of the mode instruction selects the 1/16 or 1/64 RxC rate.

The framing error flag is set if a low level is detected as the stop bit. At the end of a character, the internal parallel I/O buffer of the 8251A is fully loaded.

The RxRDY status bit indicates to the CPU that the character should be read. If read promptly, the overrun flag will not be raised, and the character will not be lost.

Figure 2H-4 RS-232 TRANSMIT AND RECEIVE CHARACTERS

2H2 Programmable Baud Rate Generator

Baud rate generator U11 provides various clock frequencies to the three programmable interface devices. U11 contains three decrementing 16-bit counters, and a command register. Counter 0 provides the RS-232/TTY clock; Counter 1 provides the sample IDee clock; and Counter 2 provides the ISE clock. The counters are programmed to operate in mode 3 to produce a square wave output.

The input clock frequency to the three down counters is 2 MHz. Multiples of the baud rate frequencies required by U8, U9, and U 10 are provided as clock inputs. The multiples are 16 and 64. To provide a baud rate of 300, for example, the 2-MHz clock is divided by 417 (decimal) which is programmed into one of the down counters in U11. This enables a clock frequency of 4800 Hz which is output to one of the 8251A devices. The 4800 Hz is then divided by 16 in the 8251A to produce a baud rate of 300.

2H3 Data Transfer to Microprocessor

The devices are addressed by the 磼 through PROM U17. The PROM generates a chip select signal so the 磼 can input data from the 8251A devices, or output data or instructions to the 8251A and the 8253 devices. Data is transferred through data transceiver U19.

2I A-C AND D-C POWER DISTRIBUTION (Refer to Figure 2I-1 and Schematic 108-C807.)

The TECHNICON RA-XT system operates on 90-125 V ac at 50/60 Hz. If required, transformer T1 can be wired to accept the following input line voltages: 100 V ac, 234 V ac, and 240 V ac at a frequency of 50 Hz or 60 Hz.

Refer to Schematic 108-C807. A-c power is applied to the primary coil of isolation transformer T1 through 12-amp circuit breaker CB1. Movister RV1 connected across the primary of T1 limits peak a-c line transients greater than 375 volts. The three windings in the transformer secondary coil produce voltages of 117 V ac, 24 V ac and 12 V ac. Fuse F1 (2.5 amps) protects the 24-V a-c line while fuse F2 (8.0 amps) protects the 12-V a-c line. Movister RV2, which is connected across the 117 V a-c secondary winding, limits peak a-c noise spikes at 150 volts. Line to line noise is reduced in the transformer secondary by RF1 power line filters FL7, FL8, and FL9.

Figure 2I-1 shows power distribution to the TECHNICON RA-XT system specific modules. Table 2-9 indicates power distribution and fuse ratings for the entire system. Refer to Schematic 108-C807 for terminal block connections.

WARNING

To avoid electrical shock hazard, shut off system power and unplug the power cord before replacing fuses, components, or modules.

Figure 2I-1 POWER DISTRIBUTION TO RA-XT MODULES

Table 2-9 A-C AND D-C POWER DISTRIBUTION

ASSY. NO.	ASSEMBLY NAME	+5	+12	+/-15	+24	+7.2	24 Va-c	117 Va-c	FUSE
A1	Reagent/Sample Dispenser	●			●			●	5A/3A
A3	Reagent Transfer	●			●				5A
A4	Sample Transfer	●			●				5A
A5	Reaction Tray	●			●				5A
A6	Reagent Turntable	●		-15				●	5A
A7	Sample Turntable	●						●	5A
A8	Colorimeter			●	●	●			
A9	Printer	●			●				5A
A10	Serial I/O PCB	●		●					
A11	Heatsink				●				
A12	Air Pump							●	3A
A13	Card Cage	●		●					
A14	CPU/Mem./Disk Ctlr. PCB	●		●					
A15	Data Acquisition PCB	●		●					
A16	Stepper Motor Ctlr. PCB	●							
A17	AC Motor Ctl. PCB	●		●					
A18	RAM Disk PCB	●		●					
A20	Reagent Probe Heater						●		
A23	Disk Drive	●	●						
A24	IDee Reader	●						●	5A
A25	Audible Alarm	●							
A26	Temperature Ctlr.						●	●	2A/5A
A31	Reaction Tray Stepper Mtr.				●				
A32	Air Injectors				●				
A33	Bar Code Reader	●							
A34	IDee Voltage Reg.			●					
A50	Indicator Panel	●							
A51	Reagent Tray Prehtr. Sw.	●						●	3A
A52	Starter/Ballast							●	
A53	Fluorescent Bracket							●	
A54	Clock Transformer							●	
A55	Touch Display							●	
A57	Reagent Tray Preheater							●	
B1-B6	Fans				●				5A

CHAPTER THREE
ALIGNMENTS & ADJUSTMENTS

WARNING

ONLY QUALIFIED SERVICE PERSONNEL WITH EXPERTISE IN ELECTRONICS, MECHANICS, HYDRAULICS, CHEMISTRY, PNEUMATICS, AND OPTICS SHOULD USE THIS MANUAL TO PERFORM THE SERVICE SPECIFIED HEREIN. LACK OF SUCH EXPERTISE MIGHT RESULT IN PERSONAL INJURY AND/OR DAMAGE TO THE SYSTEM.

TABLE OF CONTENTS

Section	Title	Page
3A	INTRODUCTION	3-1
3B	PROBE ALIGNMENTS & ADJUSTMENTS	3-1
3B1	Sample & Reagent Probe Alignment with Reaction Tray Cuvettes	3-1
3B2	Sample & Reagent Probe Alignment in Their Respective Trays	3-2
3B3	ISE Probe Alignment	3-4
3C	REACTION TRAY HOME & 90?SENSOR ADJUSTMENT	3-6
3C1	Sensor Bracket Assembly Alignment	3-6
3C2	Home & 90?Sensor Alignment	3-6
3D	FILTER WHEEL & COLORIMETER ALIGNMENT	3-9
3D1	Filter Wheel Alignment	3-9
3D2	Colorimeter Alignment	3-11
3D3	Filter Wheel Alignment Check	3-13
3D4	Procedure to Check Uniformity Among Filters	3-13
3D5	Filter Replacement Procedure	3-13
3E	PRINTER TESTS	3-16
3E1	Printer Self-test	3-17
3F	TEMPERATURE ADJUSTMENTS	3-18
3F1	Procedure to Set Reaction Tray Enclosure (Air Bath) Temperature to 30°C	3-19
3F2	Procedure to Set Reagent Probe Arm Preheater Temperature to 30癈	3-19
3F3	Temperature Verification of Liquid in Cuvette	3-20
3F4	Procedure to Set Reaction Tray Enclosure Temperature to 37癈	3-21
3F5	Procedure to Set Reagent Probe Arm Temperature to 37癈	3-21
3G	PROCEDURE TO CLEAN PROTEIN BUILDUP FROM SAMPLE PROBE	3-28
3H	TOUCH SCREEN ADJUSTMENTS	3-28

LIST OF ILLUSTRATIONS

Figure	Title	Page
3B-1	Probe Centering & Alignment in Cuvette	3-1
3B-2	Sensor Adjustment for Sample Tray	3-3
3B-3	Sensor Adjustment for Reagent Tray	3-4
3B-4	ISE Probe Adjustments	3-5
3B-5	Wash Cup Height	3-5
3C-1	Reaction Tray in Home Position	3-6
3C-2	Home & 90?Sensor Adjustment	3-7
3C-3	Sensor Disk Rotation to Align Cutouts with Sensors	3-8
3C-4	Finding Centerline of Sensor Disk Cutout	3-8
3D-1	Filter Wheel Assembly	3-10
3D-2	Filter Wheel Home Sensor Adjustment	3-10
3D-3	Filter Wheel Cutout Positioned at Centerline	3-11
3D-4	Rear View of Colorimeter Assembly	3-12
3E-1	Printer Test Sample Printout	3-16
3E-2	Proper Paper Loading	3-16
3E-3	Printer Self-test Sample Printout	3-17
3F-1	Reaction Tray Enclosure 30癈 Thermistor Sensing Circuit	3-23
3F-2	Location of Potentiometers & Switch S1	3-23
3F-3	Reagent Probe Arm Preheater 30癈 Thermocouple Sensing Circuit	3-24
3F-4a	Thermistor Routing (top view)	3-25
3F-4b	Thermistor Routing (side view)	3-25
3F-5	Reaction Tray Enclosure 37癈 Thermistor Sensing Circuit	3-26
3F-6	Reagent Probe Arm Preheater 37癈 Thermocouple	3-26
3F-7	Positioning of Air Bath Thermistor	3-27
3F-8	37癈 Temperature Profile - Cuvette #2	3-27

3A INTRODUCTION TO ALIGNMENT AND ADJUSTMENT PROCEDURES

This chapter provides the alignment procedures for various modules within the Technicon RA-XT?system. Additional alignment procedures can be found in the Product Labeling.

WARNING

Servicing areas described in this section will expose you to electrical shock hazard; therefore, only qualified personnel with expertise in electronics should perform the service procedures.

3B PROBE ALIGNMENTS AND ADJUSTMENTS

Misalignment of the sample and reagent probes can produce low chemistry results and poor reproducibility. The following procedures describe how to properly align the probes in the reaction cuvettes, sample cups, and reagent boats.

NOTE

Before aligning probes, verify that reaction tray Home and 90?sensors are properly aligned. See section 3C if alignment is necessary.

3B1 Sample and Reagent Probe Alignment with Reaction Tray Cuvettes (Refer to Figure 3B-1.)

1. Turn system power ON.
2. Load the program disk.
3. Select "UTILITIES" and home the reaction tray.
4. Loosen the clamp screw, and remove the probe arm assembly from the shaft. Remove the probe arm covers from the arms.

Figure 3B-1 PROBE CENTERING AND HEIGHT ALIGNMENT IN CUVETTE

5. Select "PROBES" and cycle the reagent probe shaft to the reaction tray dispense station.
6. Mount the reagent probe arm assembly (without cover) on the shaft over cuvette 1; but, do not tighten the clamp screw. From above, loosen the screw that secures the probe arm to the clamp, and place a 0.030-inch gauge (P/N 192-R263-01) between the shaft clamp and the probe body. Tighten the screw so that the gauge is snug.
7. Align the probe body so that it touches the cuvette tray, and the probe is centered in the cuvette. The probe arm should be parallel to the top of the cuvette.
8. Tighten the clamp screw, and remove the 0.030-inch gauge, which will drop probe body down. Tighten the screw to secure the probe body to the shaft clamp.
9. Return sample and reagent probes to the oil reservoirs.
10. Reinstall the probe arm cover on the reagent probe arm.
11. Advance the reaction tray 25 steps. Cycle the reagent probe over to the reaction tray, and observe whether the probe is touching the cuvette tray or the side of the cuvette. Repeat this step four times.
12. Using UTILITIES routine "PROBES," repeat steps 4 through 8 to align the sample probe.

NOTE

If the probe arm is set too low on the shaft it will cause the probe body to rest at an angle on top of the cuvette. The probe tip inside the cuvette also will be at an angular setting. If the probe tip is not vertically positioned in the cuvette, the sample RA fluid bubbles will not make contact with the bottom of the cuvette during dispense, and will not break up as required. Sample encapsulation then will occur producing a very low or zero chemistry result.

NOTE

Sample encapsulation will occur also if the probe arm is set too high, and the probe body does not rest on top of the cuvette.

CAUTION

The probe arm covers must not restrict the 1/8-inch free vertical movement of the probe tip.

3B2 Sample and Reagent Probe Alignment in Their Respective Trays (Refer to Figures 3B-2 and 3B-3.)

CAUTION

Sample and reagent probes must be aligned with the reaction tray cuvettes before this alignment is done.

1. Load the exerciser disk.
2. Select exerciser routine "PROBE CONTROLS" and cycle the sample probe over, but not into, the sample cup.
3. Verify that the sample probe is centered over the sample cup. Do not lower the probe into the sample cup until proper alignment is ensured.
4. If the probe is not centered, loosen the sensor bracket locking screw, and move the sensor bracket in the appropriate direction as shown in Figure 3B-2. The sensor bracket moves the sensor toward or away from the sensor hole. This causes the sample tray motor to remain on longer or stop sooner.
5. Advance the sample tray sequentially, and check alignment of the probe in each cup.

6. Exercise the reagent probe and repeat the above procedure to align the reagent probe with the reagent boats. Refer to Figure 3B-3 when adjusting the reagent tray sensor bracket.

NOTE

Inaccurate reagent aspiration will result if the reagent probe arm is set too low during alignment with the reaction cuvette. Also, a reagent probe set too low will make contact with the bottom of the reagent boat and become damaged.

NOTE

When the sample probe tip contacts the side of the sample cup, a small amount of RA fluid is rubbed off into the cup. If another aspiration is made from this same sample cup, a small amount of the dislodged RA fluid will be aspirated with sample. A lower than expected reading will be obtained for this aspiration.

Figure 3B-2 SENSOR ADJUSTMENT FOR SAMPLE TRAY

Figure 3B-3 SENSOR ADJUSTMENT FOR REAGENT TRAY

3B3 ISE Probe Alignment (Refer to Figures 3B-4 and 3B-5.)

1. Remove the ISE Probe Assembly from the transfer mechanism.
2. Using the program disk "UTILITIES" screen, select "EXERCISER," and home the reaction tray.
3. Select "ISE PROBE," and press "ENTER" repeatedly until the ISE transfer mechanism is down in the reaction tray position.
4. Refer to Figure 3B-4, and loosen screws ②.
5. Reinstall the ISE Probe Assembly. Adjust setscrew ① to align the probe vertically in the cuvette.
6. Manually rotate the ISE Probe Assembly until the probe is centered in the cuvette. Tighten screws ② .
7. Cycle the ISE probe over, but not into, the wash cup. Verify that the probe is centered over the cup. If necessary, loosen screws ③ and ④, and slide the bracket horizontally to center the wash cup under the probe.
8. Verify that the top of the wash cup is level with the top of the support bracket as shown in Figure 3B-5. Screws ⑤ in Figure 3B-4 are used for this adjustment.

Figure 3B-4 ISE PROBE ADJUSTMENTS

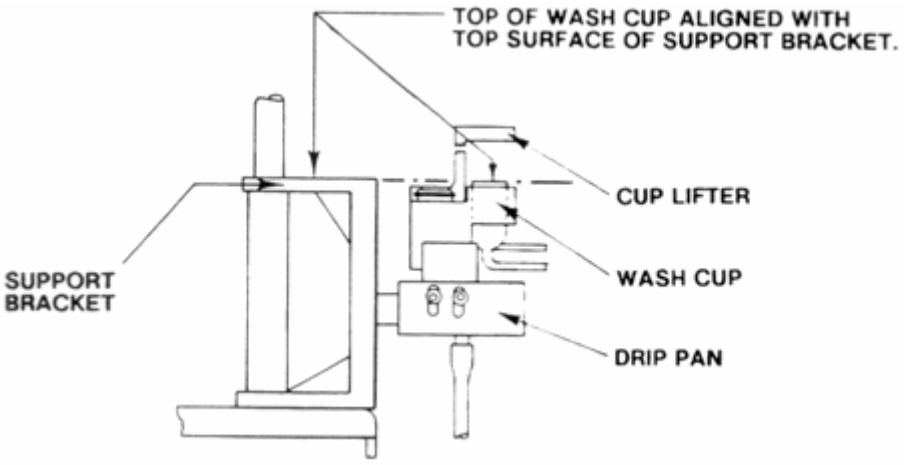


Figure 3B-5 WASH CUP HEIGHT

3C REACTION TRAY HOME AND 90?SENSOR ADJUSTMENT (Refer to Figures 3C-1, 3C-2, 3C-3, and 3C-4.)

Proper alignment of the reaction tray home and 90?sensors is critical to system operation. The alignment procedures are described in the following sections.

3C1 Sensor Bracket Assembly Alignment

Align the sensors with Alignment Tool P/N 192-R185-01 to place the sensors within 0.010 inch of the horizontal axis passing through the shaft center. This places the home and 90° sensors exactly 180?apart. Alignment should be rechecked whenever the sensor bracket assembly is replaced.

3C2 Home and 90?Sensor Alignment

The following test equipment is required for this procedure:

- Alignment pin (0.188 in: DIA by 2.5 in. long)-Technicon P/N 557-4061-01, or Winfred M. Berg P/N S3-25.
- Dual trace oscilloscope.

1. Remove the reaction tray cover, tray locking knob, and cuvette tray from the reaction turntable assembly.
2. Turn system power ON.
3. Place the 0.188-inch DIA alignment pin in the alignment hole shown in Figure 3C-1, and align the sensor disk. Ensure that the alignment pin is seated in the hole in the base assembly.

Figure 3C-1 REACTION TRAY IN HOME POSITION

NOTE

With the alignment pin in place, the drive plate should position the sensor disk cutouts close to the home and 90?sensors (as shown in Figure 3C-2) and the center of cuvette 36 almost in line with the center mark on the colorimeter.

4. Remove alignment pin, and load the program disk. Select "UTILITIES," and home the tray. "HOME POSITION" should be displayed on the screen.

NOTE

"HOME POSITION" indicates that the home stepper phase windings are energized. It is not a home sensor indicator.

5. Install the reaction tray on the drive assembly. The coarse positioning of the sensor disk (Step 3 above) placed cuvette 36 almost on the optical centerline of the colorimeter.
6. Monitor the home and 90?sensors by connecting an oscilloscope to the Stepper Motor Sensor Control Board as shown in Figure 3C-2. Connect the probe for channel A to terminal E10, and connect the probe for channel B to terminal E13. Select 5 volts/division for each channel.

Figure 3C-2 HOME AND 90?SENSOR ADJUSTMENT

7. Step the reaction tray until the center of cuvette 36 is aligned with the centerline of the colorimeter. Verify that "HOME POSITION" is displayed on the screen. If it is not, step the tray one or two half-steps to either side of cuvette 36 (see Figures 3C-3 and 3C-4). When "HOME POSITION" appears on the screen, all calibration will be done on this stepper phase. Cuvette 36 will now be off the optical center line of the colorimeter. Adjust the reaction tray by loosening the three screws securing the sensor disk to the drive plate. Reposition cuvette 36 back at the centerline of the colorimeter optics. Tighten the screws.
8. Verify that the home and 90?sensor scope traces simultaneously indicate 4.8 to 5.0 volts. If they do not, loosen the sensor bracket holding screw shown in Figure 3C-1, and adjust the bracket until both sensors simultaneously indicate 4.8 to 5.0 volts.
9. To determine if the home and 90?sensors are in the center of the sensor disk cutouts, single step the disk counterclockwise. Observe at which step the 5-volt level drops out. Return to the starting point and single step the disk clockwise. Observe at which step the 5-volt level drops out. When the sensors are properly centered there should be four half-steps on one side and three half-steps on the other side, as shown in Figure 3C-4.
10. If the home and 90?sensors are not centered, readjust the sensor bracket until the home and 90?sensors are properly aligned, then retighten the sensor bracket screw.

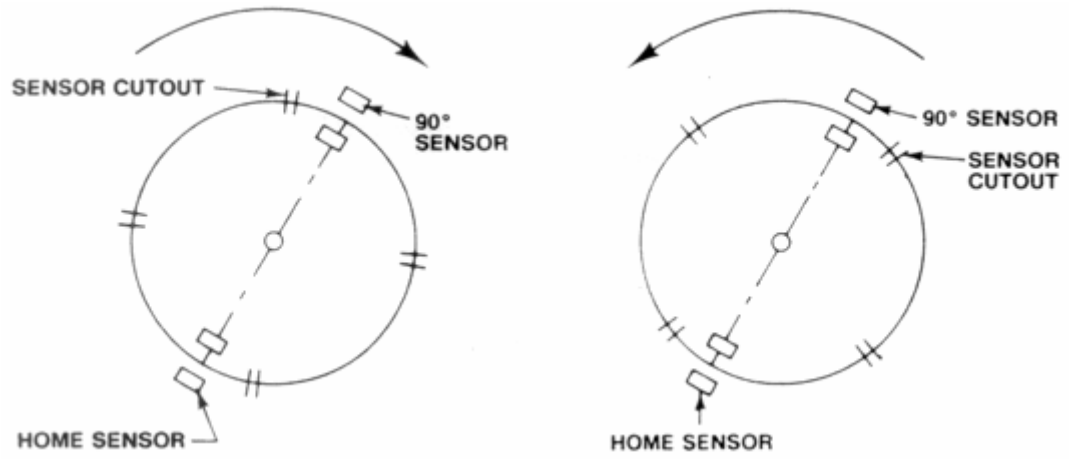


Figure 3C-3 SENSOR DISK ROTATION TO ALIGN CUTOUTS WITH SENSORS

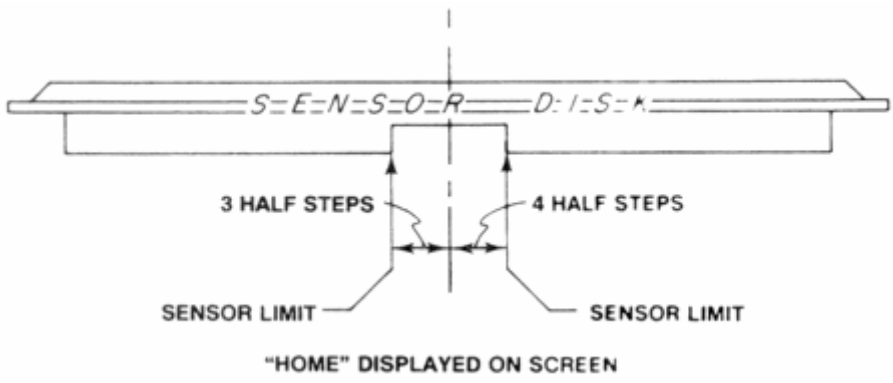


Figure 3C-4 FINDING CENTERLINE OF SENSOR DISK CUTOUT

3D FILTER WHEEL AND COLORIMETER ALIGNMENT (Refer to Figures 3D-1, 3D-2, and 3D-3.)

The following test equipment is required for this procedure:

- Alignment pin (0.062 in. DIA by 3.0 in. long)-Technicon P/N 557-4015-01, or Winfred M. Berg P/N S1-2.
- Digital Voltmeter.

3D1 Filter Wheel Alignment

1. Turn system power OFF.
2. Remove the reaction tray knob, and lift out the reaction tray.
3. Disconnect cables from the stepper motor sensor board, optics lamp, and photodetector board assemblies. Disconnect the sample and reference coax cables, and remove the cables from their mounting clips.
4. Loosen the four screws securing the colorimeter assembly.
5. Carefully slide the colorimeter assembly out from the reaction tray enclosure.
6. From the photodetector side of the colorimeter, loosen the four screws holding the stepper motor in place. Slide the stepper motor upward to disengage the motor drive pulley from the drive belt. Lock the stepper motor into position by retightening the stepper motor screws (see Figure 3D-1).
7. Carefully pull back the rubber gasket, and locate the alignment hole.
8. Rotate the filter wheel until Filter 1 is in the optical path. Insert the alignment pin as shown in Figure 3D-1.
9. Place the colorimeter assembly back on the mounting plate, and reconnect the sensor board cables. Do not secure the colorimeter in position at this time.
10. Turn system power ON. Load the program disk and select "ALIGN FW" from the UTILITIES menu. Home the filter wheel motor, and verify that "HOME" is displayed on the CRT.
11. Remove the alignment pin. Loosen the screws holding the stepper motor in position and allow it to reengage the belt. Observe whether the alignment pin aperture shifts position. If it does not, lock the stepper motor into place. If Filter 1 does shift, disengage the stepper motor from the belt, insert the alignment pin, and single-step the motor until "HOME" is again displayed on the CRT. Reengage the stepper motor with the belt. Repeat until no shifting of the alignment pin aperture is observed when the stepper motor engages the belt.
12. Monitor the sensor output signal by connecting the positive lead of the DVM to terminal E10, and the negative lead to terminal E11 (GND) on the sensor control board (see Figure 3D-2).
13. Verify that the sensor output indicates 4.8 to 5.0 volts. If it does not, turn the sensor adjustment screw clockwise or counterclockwise until a 4.8- to 5.0-volt level is observed. The adjustment screw is spring loaded, and is located behind the colorimeter mounting plate (see Figure 3D-2).

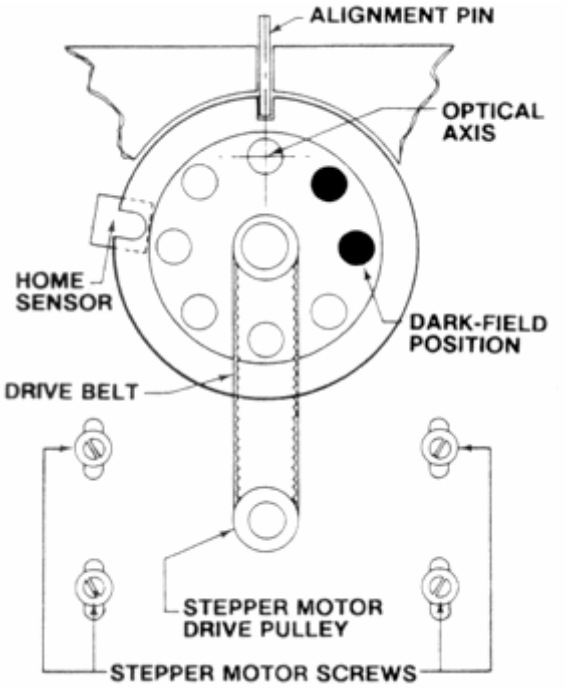


Figure 3D-1 FILTER WHEEL ASSEMBLY

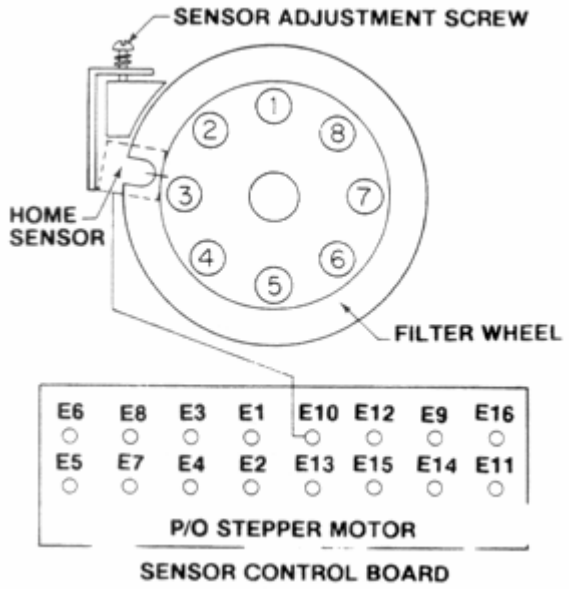


Figure 3D-2 FILTER WHEEL HOME SENSOR ADJUSTMENT

14. To determine if the sensor is aligned with the center of the sensor cutout, home the filter wheel, and verify that "HOME" is displayed on the CRT. Single-step the motor counterclockwise. Observe at which step the 5-volt level drops out. Return to the starting point, and single-step the motor clockwise until the 5-volt level drops out. When the sensor is properly centered, there will be two steps on either side of the home position. Adjust the sensor until centered as shown in Figure 3D-3.

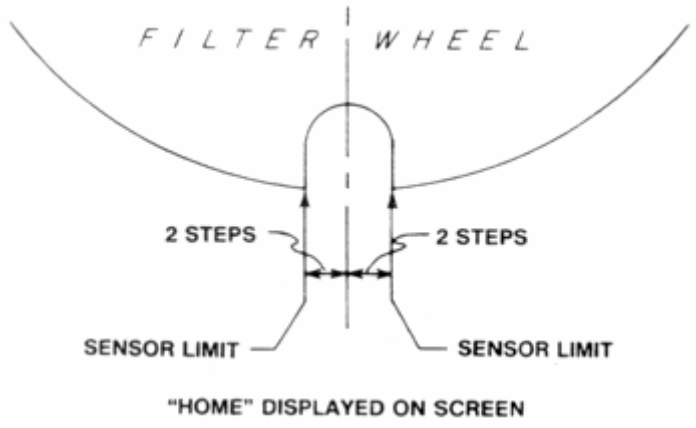


Figure 3D-3 FILTER WHEEL CUTOUT POSITIONED AT CENTERLINE

15. Shut OFF system power, and reinstall the colorimeter in the reaction enclosure. Reconnect all cables and secure source lamp housing in position.

3D2 Colorimeter Alignment (Refer to Figure 3D-4.)

NOTE

Before proceeding, make a photocopy of the *Colorimeter Data Sheet* attached at the end of section 3D.

1. With the system power OFF, loosen the screws that secure the colorimeter to the mounting plate. Slide the colorimeter out far enough so that the bias and gain pots on the photodetector boards are accessible.
2. Turn system power ON, and load the exerciser disk. Prior to making any adjustments on the photodetector boards, verify that the optics lamp voltage is 7.2 V d-c, measured at the colorimeter lamp terminal block.
3. Construct a "tunnel" with electrical tape to block out room light from the colorimeter cuvette well (see Figure 3D-4.)
4. Connect a DVM to the reference coax cable output when making adjustments to the reference photodetector board; and to the sample coax cable output when adjusting the sample photodetector board. If the colorimeter is disconnected from the system chassis, ground the colorimeter chassis to the system chassis before adjusting.
5. **Bias Adjustment:** Select exerciser test "COLORIMETER." Select Filter 7 to read dark current. Refer to Figure 3D-4 and turn gain pots R4 on the sample and reference photodetector boards fully clockwise. Adjust bias pot R2, to read 15 mV for the sample and reference channels.
6. **Gain Adjustment:** Index the filter wheel to Filter 1. Set R4 on the sample amplifier for an indication between 4.5 and 7.5 V d-c. Record the DVM reading in the "Initial" column of the *Colorimeter Data Sheet* at the end of this section.
7. Index the filter wheel to Filter 2. Record the DVM reading in the "Initial" column of the *Colorimeter Data Sheet.*

Figure 3D-4 REAR VIEW OF COLORIMETER ASSEMBLY

8. Repeat for Filters 3 through 6. Record the DVM reading for each filter in the "Initial" column of the *Calorimeter Data Sheet.*
9. If the highest recorded voltage is less than 8.8 V, or greater than 9.0 V, index the filter wheel to the position that indicated the highest voltage. Adjust R4 on the sample amplifier board for an indication of 9.0 V d-c on the DVM. Record the adjusted voltage in the "Adjusted" column of the *Colorimeter Data Sheet.*
10. Starting with Filter 1, record the adjusted voltage readings for all seven filter positions.
11. Repeat Steps 4 through 10 for the reference channel. Record the DVM readings on the *Colorimeter Data Sheet.* Leave a copy of the data sheet in Section 6 of the *Product Labeling.*
12. Remove the tape previously used to construct the "tunnel." Reinstall the Colorimeter.
13. Place a new reaction tray and cover on the system.
14. Select "A/D CONVERTER" to check the performance of the data processing function.

15. For each filter, record the Sample and Reference counts in Chart 5-8 contained in the *Test Module* section of the *Product Labeling.* The range of counts should lie approximately between 8,000 (4.8 V) and 15,000 (9.0 V). (There are 1666.7 ?% counts/volt.)

3D3 Filter Wheel Alignment Check

1. Turn system power OFF and remove the reaction tray.
2. Loosen the screws securing the colorimeter. Pull the colorimeter back from the enclosure opening so the alignment tool can be inserted into the alignment hole. DO NOT INSERT THE ALIGNMENT TOOL AT THIS TIME.
3. Turn system power ON, load the program disk, and home the filter wheel. When the filter wheel is homed, Filter 1 should be centered in the colorimeter light path.
4. Insert the alignment tool into the alignment hole. If the filter is aligned properly, the tool will seat itself completely to the stop. If it does not, the filter wheel must be realigned as described in section 3D1.

3D4 Procedure to Check Uniformity Among Filters

1. Turn system power OFF. Connect the DVM lead to the reference coax cable output.
2. Fill a cuvette with water, and position the tray so the cuvette is in front of the colorimeter.
3. Turn system power ON. Load the exerciser.
4. Select exerciser routine "COLORIMETER FILTER POSITION" and step the filter wheel to each of the six filter positions. The reference detector output signal should not exceed 9.0 volts nor be less than 4.8 volts at any position.
5. Repeat the procedure for the sample detector output signal.

3D5 Filter Replacement Procedure

NOTE

Filters must be replaced as a set. The part number of the filter set is P/N 192-R211-01.

1. Make a photocopy of the *Colorimeter Data Sheet* attached at the end of this section.
2. Shut OFF system power, and unplug the power cord.
3. Remove the colorimeter, and place it on a clean work surface.
4. Remove the two screws (180?apart) that secure the grey half of the Filter Wheel Assembly to the black half.
5. Rotate the grey half so that the large hole is over the filter to be removed. If the grey half does not rotate, do not force it. The colorimeter must be replaced.
6. Using a hemostat, remove the filter. Note which side of the filter faces in (indicated by an arrow).
7. Record on the *Colorimeter Data Sheet* the date code of the filter. The date code follows the part number.

Example: DR-DEA 108-B091-01B 44-2 (44th week of 1982)

VENDOR PART NUMBER DATE CODE

8. Record the energy value of the filter. This number appears on the filter package.

   Example: 116-Filter Lot Number
   340 nm-Filter Wavelength
   .250-Filter Energy Value

NOTE

All filter energy values must be within 10% of the 340-nm filter value.

9. Using a hemostat, insert the replacement filter into the filter wheel.
10. Repeat steps 6 through 9 for the remaining filters.
11. Remove from the filter package the orange dot that identifies the filter set number. Place the dot in a prominent location on the colorimeter.
12. Insert and tighten the two screws (removed in step 4) in the Filter Wheel Assembly.
13. Reinstall the colorimeter.
14. Realign the colorimeter as described in section 3D2.

COLORIMETER DATA SHEET

			SAMPLE		REFERENCE		
FILTER	**DATE CODE**	**ENERGY VALUE**	**INITIAL**	**ADJUSTED**	**INITIAL**	**ADJUSTED**	
1							**ADJUSTED RANGE IS 4.8 V MIN. TO 9.0 V MAX. FOR FILTERS 1 THROUGH 6.**
2							
3							
4							
5							
6							
7							**SET TO 15 mV INITIALLY**

INSTITUTION:_____ **SERIAL NO.:**_____

CUSTOMER REP.:_____ **DATE:**_____

3E PRINTER TESTS

There are no adjustments for the RA-XT thermal printer. To check print quality, select exerciser test "THERMAL PRINTER." This test prints out a full character set (Figure 3E-1). If the print quality is poor or nonexistent, verify that the paper is properly loaded as shown in Figure 3E-2.

NOTE

Failure to return the platen release lever to the engaged position prevents data transmission to the printer.

Figure 3E-1 PRINTER TEST SAMPLE PRINTOUT

Figure 3E-2 PROPER PAPER LOADING

3E1 Printer Self-test

Execute the printer self-test after checking the paper and the platen release lever.

1. Shut off system power.
2. Disconnect the ribbon cable from connector CN1 on the Printer Controller Board. Connect CN1 pin 29 (FEED) to CN1 pin 30 (GND).

NOTE

Pin connections must be made with the system power off. Initialization then will occur on system power up. A system reset will not initialize the change.

3. Apply power to the system. The printer will print the test pattern shown in Figure 3E-3.
4. Shut off system power to terminate the test.

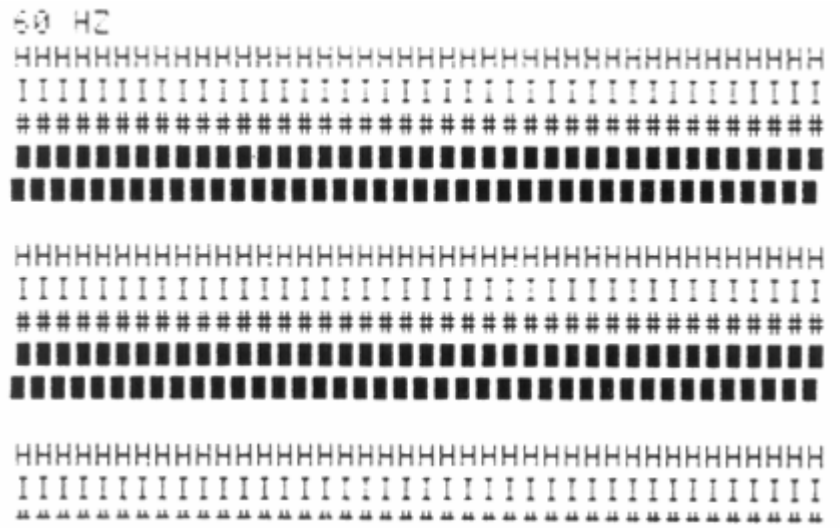


Figure 3E-3 PRINTER SELF-TEST SAMPLE PRINTOUT

3F TEMPERATURE ADJUSTMENT PROCEDURES

NOTE

Figures referenced in the procedures are contained at the end of section 3F.

The goal of the temperature control system is to bring the temperature of the liquid in each cuvette up to the proper temperature, and to maintain the temperature within range over the length of the reaction. In the case of 37癈 chemistries, the range is 36.8癈 to 37.2°C.

The following temperatures should be set when a new temperature controller is installed: Reaction tray module enclosure (to 30癈 or 37癈), reagent probe preheater (to 30癈 or 37癈), temperature of liquid in cuvette, and reaction chamber temperature (air bath). These procedures involve many steps and are time consuming. They may take two or three hours to complete. Therefore, do not perform them unless absolutely necessary. 37癈 adjustments may be made as needed.

Test Equipment Required:

a. Yellow Springs Instruments 45 CU thermometer and 4502 thermistor probe.

b. Modified reaction tray cover P/N 108-B349-02 or 192-R540-01 (this is a regular reaction tray cover with a 1/8-inch hole in the middle, and a special antievaporation shield).

c. Used sample probe (P/N 108-0925-01).

d. Used reagent probe (P/N 108-0967-01).

NOTE

Although damaged sample and reagent probes may be used, they must not be occluded, and they must be able to deliver proper volumes of sample and reagent.

Preliminary Checks:

a. Verify that the air bath thermistor is at the proper height. (Refer to figure 3F-7.)

b. Set aside 1/2 liter of deionized water to equilibrate to room temperature for later testing.

Procedure Guidelines:

a. To accurately gauge temperatures, install the YSI 4502 thermistor probe in cuvette #2 **ONLY.** (Refer to Figures 3F-4a and 3F-4b.)

IMPORTANT

To ensure temperature stability when performing these tests, the system cover must be closed and bolted down.

b. Monitor the temperature in cuvette #2 while running a special user-defined chemistry using water instead of reagents.

c. The requirement to be met is that 45 seconds after the addition of sample, the temperature of the cuvette must be within the range of 36.8癈 to 37.2癈, and remain within that range for the next 9.5 minutes.

d. If the temperature is incorrect after 45 seconds, but eventually levels out correctly, the reagent preheater must be adjusted.

e. If the temperature is correct after 45 seconds, but eventually levels out incorrectly, the air temperature must be adjusted.

NOTE

Although damaged sample and reagent probes may be used, they must not be occluded, and they must be able to deliver proper volumes of sample and reagent.

3F1 Procedure to Set Reaction Tray Enclosure (Air Bath) Temperature To 30癈 (Refer to Figure 3F-1.)

NOTE

Any alteration of 30癈 settings will alter the 37癈 settings. For best results, perform this procedure at a room temperature midrange to the temperatures normally experienced in the lab.

1. Turn system power off, and remove the reaction cover and tray. Check the thermistor tip position. (Refer to Figure 3F-7.)
2. Set switch S1 on the temperature controller assembly to the 37癈 position. Refer to Figure 3F-2 for switch and potentiometer locations.
3. Adjust temperature set potentiometer R3 on PCB 108-B303 to 3100 ? ohms (30.00癈 ?.05癈). Read the resistance across pins 1 and 2 of the potentiometer. (Refer to Figure 3F-3.)
4. Set switch S1 on the temperature controller assembly to the 30癈 position. Adjust temperature set potentiometer R4 on the temperature controller to balance a 2391 ?5 ohm resistance at a 25癈 ambient temperature setting. Read the resistance across the potentiometer. (Refer to Figure 3F-6.)
5. Pass the YSI 4502 thermistor probe through the same sensor cable opening as that used for the instrument thermistor cable.
6. Position the 4502 probe within 1/4 inch of the reaction tray thermistor. Use an elastic band if necessary to hold the probe in place. Make sure that the probe wire does not come into contact with the heater coil.
7. Connect the 4502 probe to the YSI 45 CD thermometer.
8. Verify that the air bath thermistor tip is 1 inch from the top of the thermistor holder. (Refer to Figure 3F-7.)
9. Place the reaction tray, and sample and reagent tray covers on the system.
10. If the reaction module enclosure is not in the 30.1癈 to 31.4癈 range at 25癈 ambient, readjust set potentiometer R26 on Temperature Controller 1. (R26 on Temperature Controller 1 is the upper potentiometer on the left-hand side of the instrument.) Allow at least five minutes for the temperature to stabilize after each potentiometer adjustment.

NOTE

One quarter turn of the potentiometer changes the temperature approximately 0.2癈. CW increases air bath temperature. CCW decreases air bath temperature.

3F2 Procedure to Set Reagent Probe Arm Preheater Temperature to 30癈 (Refer to Figure 3F-3.)

NOTE

Any adjustment made to the 30癈 setting will affect the reagent probe arm preheater. The procedure to set the reaction module enclosure to 30癈 must be performed prior to setting the reagent probe preheater temperature.

1. Perform the procedure contained in Section 3F3.
2. If the temperature of cuvette #2 is not between 29.8癈 and 30.2癈 forty-five seconds after the sample is added, adjust potentiometer R26 on Temperature Controller 2. R26 on Temperature Controller 2 is the lower potentiometer on the left-hand side of the instrument. (Refer to Figure 3F-3.)

NOTE

One revolution of the potentiometer equals approximately a 0.2癈 change. CW increases air bath temperature. CCW decreases air bath temperature.

3F3 Temperature Verification of Liquid in Cuvette

NOTE

It is important that only cuvette #2 be used for liquid temperature measurements. Note also that a loop of wire extending to cuvette #9 (approximately 3 inches) must be taped to the underside of the cuvette tray as shown in Figures 3P-4a and 3F-4b.

Since it is necessary to drill two 1/8-inch holes in the cuvette tray, and to plug these holes after the thermistor is routed through, it is recommended that the modified cuvette tray and test cover be left intact (with thermistor) for use on other systems. Use RTV or PARAFILM* to seal the 1/8-inch holes.

Tray test cover P/N 192-R540-01 or 108-B349-02 is to be used when performing this procedure.

1. Place the YSI 4502 thermistor probe in cuvette #2. (Refer to Figures 3F-4a and 3F-4b.) Plug the probe wire into the YSI 45 CD thermometer.
2. Install the used sample and reagent probes.
3. Fill sample cup numbers 1, 2, and 3, and reagent boat number 1 with deionized water equilibrated to room temperature.
4. Using the USER CHEMISTRY screen, set up a user defined chemistry with the following parameters:

TYPE	ENDPOINT
% SAMPLE VOLUME**	30
WAVELENGTH	340
DELAY TIME**	9:30
% REAGENT VOLUME**	72
UNITS	MG/DL
UNIT FACTOR	1
DECIMAL POINT	0
RBL LOW	0
RBL HIGH	1
RANGE LOW	0
RANGE HIGH	100
CALIBRATION FACTOR	1
STANDARD VALUE	1
NORMAL LOW	1
NORMAL HIGH	2
SLOPE	1
INTERCEPT	0
ENDPOINT LIMIT	1

NOTE

After the last entry, the above parameters will be printed out automatically.

5. Assign the user-defined chemistry to reagent boat 1. Program a worklist of three cups using the OPERATE screens.
6. During operation, observe the temperature reading for cuvette number 2. Forty-five seconds after the sample is dispensed, the cuvette must be within 30.0癈 ?.20癈 or 37.0癈 ?.20癈. The temperature must

remain within these limits for the next 9.5 minutes. (Refer to Figure 3F-8.)

7. If the requirements of step 6 are not met, adjust either the reagent preheater or the air bath. (Refer to Figure 3F-8.) Wait 5 minutes between adjustments.

IMPORTANT

The system cover must be closed while performing this test. Lift the cover no more than 12 inches to adjust the temperature controller.

8. Using a narrow pipette, remove the water from reaction cuvettes 1, 2, and 3. Allow the thermistor probe to recover to greater than 36.5癈 (cuvette air temperature) before proceeding. (All of the water must be evaporated before the cuvette will come up to temperature.)
9. From the "UTILITIES" screen, select "EXERCISER," and home the reaction tray. Reposition cup #1 in front of the bar code reader. Use the "OPERATE" screens to program a new worklist.
10. Repeat steps 6 through 9 after each adjustment until step 8 is satisfied.
11. If this procedure is being performed in response to a customer chemistry complaint (especially an enzyme test), repeat steps 5 through 9 running the "complaint" chemistry. Use water for sample and reagent. Make temperature adjustments accordingly.
12. Inspect the tips of the original probes for damage. Discard if damaged. Reinstall the original or replacement probes.
13. When finished, bolt down the system cover securely with the two bolts under the cover in the front.

3F4 Procedure to Set Reaction Tray Enclosure Temperature to 37癈 (Refer to Figure 3F-5.)

NOTE

During the initial setting of temperatures, the 30癈 and 37癈 settings must both be made. Adjustments made to 30癈 settings will affect the 37癈 settings. However, adjustment made to the 37癈 settings will not affect the 30癈 settings.

1. Verify proper reaction chamber thermistor height. (Refer to Figure 3F-7.)
2. Set switch S1 to the 37癈 position. Place the reaction tray and cover on the system. Wait 20 minutes for the temperature to stabilize.
3. If the temperature of the reaction module enclosure is not in the 37.1癈 to 39.0癈 range, adjust air temperature potentiometer R1 (right-hand pot) located on the temperature controller mounting plate.

IMPORTANT

Allow five minutes after each potentiometer adjustment for the temperature to stabilize.

NOTE

One revolution of the potentiometer equals approximately a 0.2癈 change. CW increases air bath temperature. CCW decreases air bath temperature.

3F5 Procedure to Set Reagent Probe Arm Temperature to 37癈 (Refer to Figure 3F-6.)

NOTE

If the system is run at both temperatures, the 30癈 setting for the reaction chamber and reagent preheater must be performed prior to making the 37癈 adjustment. However, 37癈 adjustments can be made without first making 30癈 adjustments if the system is run at 37癈 only.

1. Perform the procedure contained in Section 3F3.
2. If the temperature of cuvette #2 is not between 36.8癈 and 37.2癈 forty-five seconds after the sample is

added, adjust potentiometer R2 on the temperature controller mounting plate. (Refer to Figure 3F-6.)

IMPORTANT

When deciding on which adjustments to make, keep the reagent preheater as cool as possible while meeting the temperature requirements. Excessively preheated reagent and sample may adversely affect the enzyme tests.

NOTE

One revolution of the potentiometer equals approximately a 0.2癈 change. CW increases air bath temperature CCW decreases air bath temperature.

Figure 3F-1 REACTION TRAY ENCLOSURE 30°C THERMISTOR SENSING CIRCUIT

Figure 3F-2 LOCATION OF POTENTIOMETERS AND SWITCH S1

Figure 3F-3 REAGENT PROBE ARM PREHEATER 30°C THERMOCOUPLE SENSING CIRCUIT

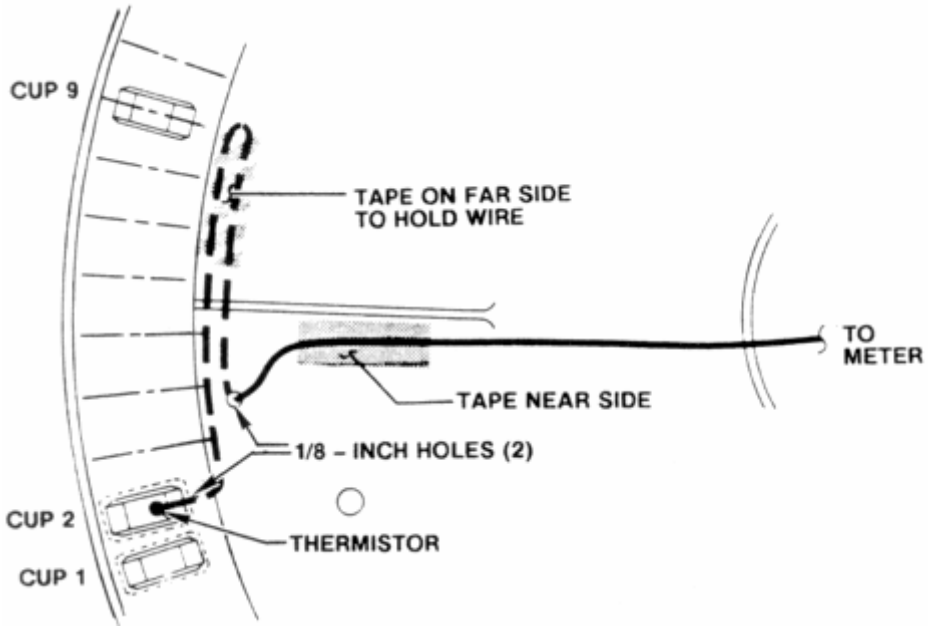


Figure 3F-4a THERMISTOR ROUTING (TOP VIEW)

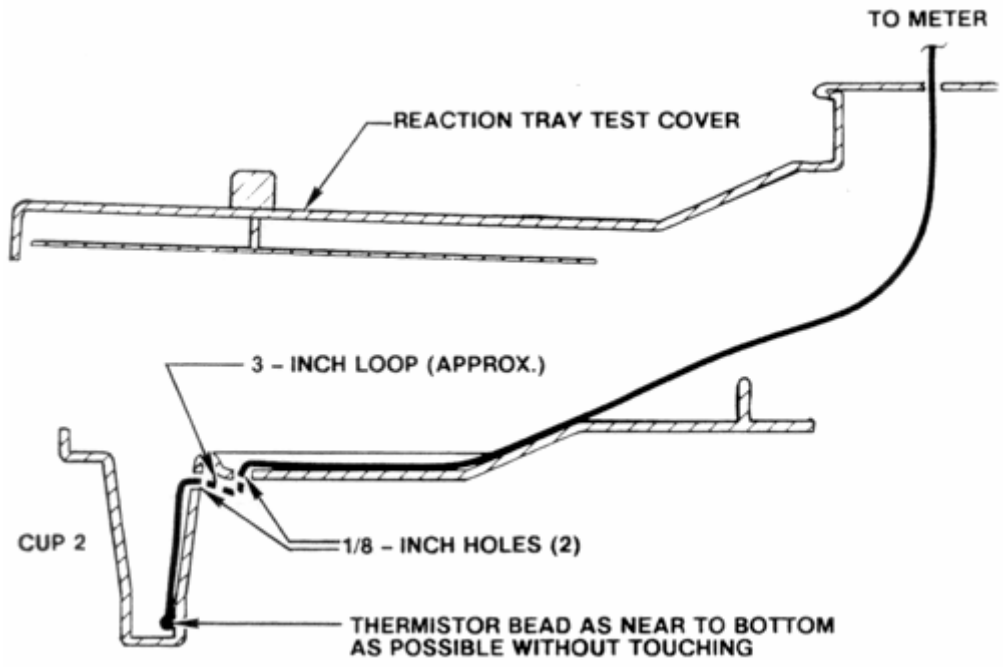

TO METER
REACTION TRAY TEST COVER
3 – INCH LOOP (APPROX.)
CUP 2
1/8 – INCH HOLES (2)
THERMISTOR BEAD AS NEAR TO BOTTOM
AS POSSIBLE WITHOUT TOUCHING

Figure 3F-4b THERMISTOR ROUTING (SIDE VIEW)

Figure 3F-5 REACTION TRAY ENCLOSURE 37°C THERMISTOR SENSING CIRCUIT

Figure 3F-6 REAGENT PROBE ARM PREHEATER 37°C THERMOCOUPLE

Figure 3F-7 POSITIONING OF AIR BATH THERMISTOR

Figure 3F-8 37°C TEMPERATURE PROFILE - CUVETTE #2

3G PROCEDURE TO CLEAN PROTEIN BUILDUP FROM SAMPLE PROBE

1. Using a Kim Wipe, remove residual RA fluid from the sample probe.
2. Immerse the probe in a 5% solution of sodium hypochlorite (liquid bleach substitute) for up to one half hour. DO NOT ALLOW THE ALUMINUM PORTION OF THE PROBE TO COME INTO CONTACT WITH THE BLEACH.
3. Wipe the bleach off the probe with a Kim Wipe. The purpose of this cleaning is to remove all proteinaceous material from the outside of the probe.
4. Rinse the probe with distilled water.
5. Prime with RA fluid before using the probe. This should be done every two weeks, assuming eight-hour-a-day operation.

NOTE

In order to correct the "egg" forming problem, perform the probe alignment procedures also.

3H TOUCH SCREEN ADJUSTMENTS

Touch screen preformance tests, video alignment, and calibration procedures are contained in Section 6 of the Fluke 1780A Instruction Manual. Some of these procedures require manipulation of the control switches at the rear of the module. The normal settings of the switches for use with the RA-XT system are as follows.

Switch Sl:

POSITION	SETTING	FUNCTION
1	Down	No Parity
2	Down	Odd/Even
3	Down	1 Stop Bit
4	Up	8 Data Bits
5	Down	Test Mode OFF
6	Down	Auto LF OFF
7	Down	Auto Wrap-Around OFF

Switch S2:

Position 7 = 9600 Baud Rate

CHAPTER FOUR
ISE MODULE

WARNING

ONLY QUALIFIED SERVICE PERSONNEL WITH EXPERTISE IN ELECTRONICS. MECHANICS, HYDRAULICS, CHEMISTRY, PNEUMATICS, AND OPTICS SHOULD USE THIS MANUAL TO PERFORM THE SERVICE SPECIFIED HEREIN. LACK OF SUCH EXPERTISE MIGHT RESULT IN PERSONAL INJURY AND/OR DAMAGE TO THE SYSTEM.

TABLE OF CONTENTS

Section	Title	Page
4A	SYSTEM DESCRIPTION	4-1
4A1	Operational Sequence	4-1
4A2	Analytical Processing	4-2
4A3	Sample Results Processing	4-4
4A4	Baseline Adjust, Drift, and Range Checks	4-4
4A5	Pump/Electronics Module	4-5
4A5.1	Reagent Pump Assembly	4-5
4A5.2	ISE Display Board	4-6
4A5.3	Air Pump and Air Injector Solenoids	4-6
4A6	ISE Assemblies Located in RA-XT System	4-6
4A6.1	Sample Transfer Mechanism	4-6
4A6.2	Analytical Electrode Assembly	4-6
4B	DETAILED FUNCTIONAL DESCRIPTIONS	4-11
4B1	Analytical Electrode Assembly	4-11
4B1.1	Electrode Selectivity	4-11
4B2	Two-point Calibration	4-14
4B3	Signal Processing and Data Acquisition	4-15
4B3.1	ISE Amplifier Board	4-15
4B3.2	Preamp Circuits	4-16
4B3.3	Amp Adjust Circuit	4-17
4B3.4	A/D Converter Board	4-17
4B3.4.1	Circuit Description	4-17
4B3.5	Data Acquisition Board	4-18
4B3.5.1	Circuit Description	4-18
4B4	Air Injection	4-21
4B4.1	Air Injection Control Board	4-21
4B5	Sample and Reagent Delivery	4-21
4B5.1	Circuit Description	4-22
4B5.1.1	8741A CPU	4-22
4B5.1.2	Stepper Motor Sensor Board	4-22
4B6	ISE Display Board	4-23
4B6.1	Circuit Description	4-23
4B7	ISE Sample Transfer Mechanism	4-24
4B8	RA-XT System/ISE Module Interface	4-24

4B8.1	USART Description	4-25
4B9	Program Downloading	4-25
4B9.1	Downloading Messages	4-25
4B10	RA-XT System Software Control of ISE Functions	4-26
4B11	ISE Pump/Electronics Module Operational States	4-26
4B12	ISE CPU Functions	4-28
4B12.1	Detailed Description	4-28
4B13	Power Distribution	4-29
4B13.1	A-c Input Voltage Selection	4-29
4B13.2	Circuit Description	4-29

LIST OF ILLUSTRATIONS

Figure	Title	Page
4A-1	ISE Dispense and Aspirate Positions	4-2
4A-2	ISE Operational Sequence	4-3
4AFO1	ISE Module Interfaced with RA-XT System	4-9
4B-1	Simplified Diagram of ISE Measuring System	4-11
4B-2	CO_2 and K Electrode Assemblies	4-12
4B-3	Na Electrode Assembly	4-12
4B-4	Reference Electrode Assembly	4-12
4B-5	ISE Analytical Module	4-13
4B-6	Simplified Diagram of ISE Amplifier Circuit	4-15
4B-7	Data Processing Timing Diagram	4-20
4B-8	ASCII Display Characters	4-23
4B-9	Operational State Flowchart	4-27
4B-10	Voltage Selector Module	4-30
4B-11	Voltage Selector Board and Schematic	4-30
4BFO1	ISE Electrode Amplifier Circuit FBD	4-31
4BFO2	A/D Converter Circuit FBD	4-32
4BFO3	Pinch Valve Control Circuit FBD	4-33
4BFO4	Stepper Motor Circuit FBD	4-34
4BPO5	ISE Display Board FBD	4-35
4BFO6	ISE Probe Transfer Mechanism Control Circuit	4-36
4BFO7	RA-XT/ISE Electronic Interface	4-37

LIST OF TABLES

Table Number	Title	Page
4-1	Printer Flag Symbols	4-4
4-2	Slope Limits	4-15
4-3	ISE Amplifier Parameters	4-16
4-4	ISE Input Control	4-17

4A SYSTEM DESCRIPTION (Refer to Figure 4AFO1.)

The Ion Selective Electrode (ISE) option to the TECHNICON RA-XT system enables analysis of serum and urine for sodium, potassium, and carbon dioxide levels. The Na/K/CO_2 tests are performed simultaneously at a sample throughput rate of 240 per hour.

The ISE option consists of three basic assemblies:

- ISE Sample Transfer Assembly 108-B458-01
- Analytical Electrode Assembly 108-B469-01
- Pump/Electronics Module 108-B400-01

The ISE Sample Transfer Assembly, two additional air injectors, and the Analytical Electrode Assembly are located in the TECHNICON RA-XT system. The pump/electronics assemblies are contained in a separate module, which is connected to the TECHNICON RA-XT system by cables and hydraulic tubing.

The ISE Transfer Assembly consists of a basic sample transfer assembly with an additional ISE probe transfer mechanism. The ISE resample probe aspirates samples requiring ISE analysis from the reaction tray, and routes them to the ISE Analytical Electrode Assembly.

The Analytical Electrode Assembly contains the ion selective electrodes and the reference electrode. The sample stream enters the Analytical Electrode Assembly at one end, and is presented to the sodium, potassium, and carbon dioxide ISEs. A KCI reference solution enters at the other end of the Analytical Electrode Assembly, and is presented to the reference electrode. The ion selective electrodes produce small electrical potentials that are proportional to the logarithm of the respective sodium, potassium, and carbon dioxide ion concentrations in the sample. The air injector assembly injects bubbles into the resample stream during resample aspiration to reduce carryover.

The Pump/Electronics Module contains the CPU Control Board, which controls the reagent pump, air valves, indicator lamps, ISE display, amp adjust signal, and resample probe mechanism. The sequence of ISE mechanical operations and sample processing are controlled solely by the ISE CPU Control Board after receiving a SAMPLE command from the TECHNICON RA-XT system. A four-character display and three indicator lamps (STARTUP, READY, and OPERATE) on the Pump/Electronics Module provide the operator with the ISE operational status.

4A1 Operational Sequence

The Pump/Electronics Module passes through three operational states before executing any commands to process samples. The states are STARTUP, READY, and OPERATE. When power is applied to the Pump/Electronics Module, it enters the STARTUP state. In this state the ISE operating program is downloaded from the TECHNICON RA-XT system, and the Pump/Electronics Module electronics are initialized. When the STARTUP conditions are acceptable, the system steps to the READY state where it is held in a standby condition to await commands from the TECHNICON RA-XT system. The commands may be: go to the OPERATE state, go to the Calibration Cycle; or go to the Diagnostic Routine. A periodic conditioning protocol also is initialized automatically in this state.

The sample or samples designated for Na, K, and CO_2 analysis are specified in the worklist, which is entered via the touchscreen display on the TECHNICON RA-XT system.

When the TECHNICON RA-XT system enters the OPERATE state, the software scans the worklist to check for ISE selections. If an ISE test was requested and a valid ISE two-point calibration is in effect, the ISE system enters the OPERATE mode.

4A2 Analytical Processing

In the OPERATE mode, the reagent probe aspirates 325 µL of buffer from the reagent tray, and dispenses it into the cuvette positioned at the dispense station.

At the same time, the ISE probe starts six repetitive cycles of aspirating wash/cal solution from the ISE wash receptacle. For these first six operating (aspirating) cycles, the ISE probe travels only in an up and down direction in conjunction with the movement of the sample probe. Each time the ISE probe returns to the wash/cal receptacle, the ISE pump is energized for approximately three seconds, thus pumping wash/cal solution into the ISE Analytical Electrode Assembly. While aspiration is taking place, air valves (V3 and V4) are turned on and off to inject seven air bubbles into the sample (wash/cal).

The software initiates eleven wash/cal readings on the fifth and sixth wash/cal samples. These readings are used to make the following checks and adjustments: Baseline Adjust, Drift Check, and Range Check. (If a two-point calibration is performed, then wash/cal readings one and two are used to set the AMP voltage, and to verify the proper voltage setting).

The cuvette containing the first aspiration of reagent buffer arrives at the sample dispense station four operating cycles after the OPERATE state is entered (see Figure 4A-1).

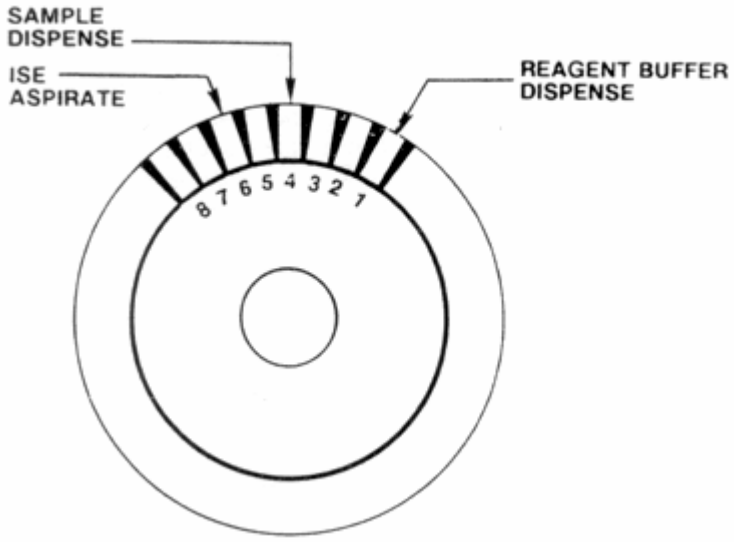


Figure 4A-1 ISE DISPENSE AND ASPIRATE POSITIONS

The sample probe aspirates 25.0 µL of sample from the first cup in the sample tray, and then dispenses it into the reaction cuvette. The mixture of sample and buffer produces a dilution ratio of 14-1 At the start of the seventh operating cycle, the first diluted sample arrives at the ISE aspirate station, as shown in Figure 4A-2. The ISE probe moves into the cuvette, and draws the diluted sample into the delay coil at the input of the Analytical Electrode Assembly.

As the sample is drawn into the delay coil tubing, seven air bubbles are injected into the sample stream by valves V3 and V4. During the next operating cycle the sample is pulled into the Analytical Electrode Assembly, where voltages proportional to the concentrations of Na, K, and CO_2 are produced.

After aspirating sample, the ISE probe leaves the cuvette and returns to the wash receptacle, where the ISE pump aspirates a two-second segment of wash/cal solution, preceded by a small volume of air that acts as a wash between samples. The ISE reagent pump also draws counterflow reference solution into the reference compartment of the Analytical Electrode Assembly.

Voltages proportional to the concentrations of Na, K, and CO_2, and a reference potential are sent to amplifier circuits on the ISE Amplifier Board. The voltages are amplified and processed on this board to meet the operating requirements of the A/D stage that follows. Eleven voltage readings are taken to determine the Na, K, and CO_2 values while the sample is in the Analytical Electrode Assembly. The eleven readings are taken over a period of about 5.5 seconds at half-second intervals.

The A/D converter changes the respective analog signals for Na, K, and CO_2 into digital signals proportional to the analog input voltage. The digital signals for each of the readings are sequentially loaded into 16-bit down counters on the Data Acquisition Board until requested by the ISE CPU Control Board.

Figure 4A-2 ISE OPERATIONAL SEQUENCE

4A3 Sample Results Processing

The ISE software performs data point sampling and averaging to determine an average end point, referred to as the Mean Count (MC). An average of four consecutive readings that have the least amount of deviation from one another are selected from the total of eleven readings to determine the Mean Count. The four consecutive readings are the read points where the electrodes are most stable during the sample read period. The average reading or Mean Count is sent to the TECHNICON RA-XT system CPU where it is compared to a stored limit. It is then determined if the most recently calculated MC is within the accepted range. If so, the MC is utilized in the calculation algorithm, which converts A/D counts into an equivalent concentration. This value is reported on the system printer. Unacceptable test results are flagged, as shown in Table 4-1.

The algorithm is as follows:

$$CONCENTRATION = log_{10} \{log\ HiCal + [(log\ LoCal - log\ HiCal)\ (MC - MHC / MLC - MHO)]\}$$

where:

MC = mean counts
MHC = mean A/D counts for ISE Calibrator High
MLC = mean A/D counts for ISE Calibrator Low
HiCal = the concentration value of ISE Calibrator High
LoCal = the concentration value of ISE Calibrator Low

A SAMPLE command is issued from the TECHNICON RA-XT system to the ISE CPU Control Board every 15 seconds. The ISE probe remains in the wash position for those samples that do not require ISE analysis. However, the ISE CPU still issues all the commands required to process a sample, in this case wash/cal solution.

TABLE 4-1 PRINTER FLAG SYMBOLS

SYMBOL	EXPLANATION
* (with value)	Reported value is out of normal range for this channel.
>300	Calculated value for Na and/or K would have been greater than 300 mmol/L.
<1	Calculated value for Na and/or K would have been less than 1 mmol/L.
# (without value)	Value is not reported because it may not be accurate due to detected curve abnormality. (There is not a flat portion of the curve for the eleven readings.)

4A4 Baseline Adjust, Drift, and Range Checks

- *Baseline Adjust Description* - A baseline adjustment is performed at the beginning of every worklist where ISEs are requested, and when a TRAY FULL condition requires continuation of a worklist on a new tray. The A/D counts for the fifth and sixth wash cycles are stored, and their difference is compared to an internal drift constant. If the difference is less than the constant, the readings for wash 5 and wash 6 are averaged and compared with the previously stored baseline average. The new/stored baseline ratio is computed and algebraically added to the Hi Cal and Low Cal set points established in the last 2-point calibration. This correction moves the Lo Cal and Hi Cal points by the same amount, and in the same direction, changing the intercept but not the slope. Unknowns that follow on each worklist are then calculated from a new corrected baseline.

- *Drift Error Description* - The readings for the fifth and sixth wash cycles are stored, and their difference is compared to an internal drift constant. If the readings are greater than the constant, the appropriate drift error message is displayed for that channel.
- *Range Error Description* - All calibrants and unknowns are checked to ensure that they fall within the 1 to 9 volt ISE amplifier range. Any value outside this range is flagged.

4A5 Pump/Electronics Module (Refer to Schematics 108-C408, 108-C432, and 108-C806.)

The Pump/Electronics Module is connected to the TECHNICON RA-XT system by power and signal cables, and hydraulic tubing. The ISE CPU Control Board, located within the Pump/Electronics Module, controls the reagent pump, air valves, indicator lamps, ISE display, ISE probe transfer mechanism, and data acquisition for ISE samples. The ISE Analytical Electrode Assembly, ISE probe transfer mechanism, and air valves are located in the TECHNICON RA-XT system. The Pump/Electronics Module consists of the following major subassemblies:

- Isolation Assembly, which houses the power transformer and line filter
- Pump Assembly, consisting of the stepper motor driven pump and stepper motor sensor board
- Power Supply Assembly, consisting of the ?4-volt power supply, the cooling fan, and the heat sink assemblies
- Card Cage, which houses the ISE CPU Control Board, and the Data Acquisition Board with the A/D Converter Board mounted on it
- Display Board, located under the front panel
- Air Pump Assembly
- Wash, Reference, and Waste containers

4A5.1 Reagent Pump Assembly

The reagent pump assembly is a four-channel peristaltic pump, which is driven by a stepper motor. One channel aspirates sample from a reaction tray cuvette, and draws it to the Analytical Electrode Assembly, located in the TECHNICON RA-XT system. The second channel pumps reference solution, from a container located in the Pump/Electronics Module, to the Analytical Electrode Assembly. The other channels pump wash solution to the wash cup, and aspirate overflow from the wash cup.

The pump consists of four rotors directly driven by a 1.8?d-c stepper motor. A spring-loaded platen compresses the pump tubes against the rotors. A stepper motor sensor board, mounted in the reagent pump assembly, converts the logic level control signals to power level drive signals required by the motor.

The reagent pump is actuated twice during each 15-second analytical cycle. The first time the pump is turned on, the ISE probe is positioned in a reaction tray cuvette. At this time, diluted sample is pumped into the delay coil. The sample, currently in the delay coil from the previous cycle, is pumped into the Analytical Electrode Assembly, and the contents of the Analytical Electrode Assembly are pumped to waste. The second time the pump is actuated the ISE probe is positioned in the wash cup. During this period, Wash/Cal solution is pumped into the delay coil, and counterflow reference solution is pumped to the Electrode Assembly.

4A5.2 ISE Display Board

The ISE Display Board is used to display messages from the ISE module and the TECHNICON RA-XT system through a four-digit LED assembly. The start-up, ready, and operate states of the ISE module are indicated when the respective incandescent lamp is illuminated.

4A5.3 Air Pump and Air Injector Solenoids

The air pump is driven by a synchronous a-c motor to produce 5 psi of pressurized air. The motor receives 115 V ac continuously for as long as the system power is turned on. The motor is coupled to the piston shaft by an eccentric. The piston delivers the 5 PSI air to a dual check valve, which allows atmospheric air to be drawn in on the down stroke, and compressed air to be released to the air injector pinch valves on the up stroke.

Air pressure can be adjusted to 5 psi by loosening the motor hold down screws, and sliding the motor up or down.

The air injector pinch valves are program controlled to inject air bubbles into the sample stream, and require 24 V dc to operate. The pinch valves, which are located in the RA-XT system, are controlled by logic level signals from the ISE CPU Control Board. Logic level signals are converted to power level drive signals on the Air Injection Control Board, located in the TECHNICON RA-XT system.

4A6 ISE Assemblies Located in the RA-XT System

Although the assemblies described below are located on the RA-XT system, they are controlled by the ISE CPU Control Board located in the ISE Pump/Electronics Module.

4A6.1 Sample Transfer Mechanism

The TECHNICON RA-XT system sample transfer mechanism contains an additional transfer assembly for the ISE resample probe. The function of the ISE resample probe is to transfer samples requiring ISE analysis from the reaction tray to the ISE Analytical Electrode Assembly.

The ISE probe is mounted on the same drive shaft as the TECHNICON RA-XT system sample probe. Both the TECHNICON RA-XT system sample probe and the ISE resample probe are driven up and down simultaneously by the same 24-V d-c motor. The ISE resample probe's horizontal motion is independent of the TECHNICON RA-XT system sample probe by the use of a free-rotation collar holding the ISE resample probe arm to the shaft. The rotation collar imparts horizontal motion to the ISE sample probe through a link provided by a cam follower arm. The cam follower arm is driven by a 24-V d-c motor controlled by the ISE CPU Control Board. A sensor disk with a signal detection slot is connected to the motor shaft also. Three optical sensors situated around the disk provide position data (wash, etch/clean, and reaction tray) to the ISE CPU Control Board.

The vertical drive commands for the TECHNICON RA-XT system probe and the ISE resample probe are issued from the AC Motor Control Board, located in the TECHNICON RA-XT system card cage. The horizontal drive command for the ISE resample probe are issued from the ISE CPU Control Board, located in the ISE module. The logic level commands are converted to power level drive signals through the respective DC Motor/Sensor Control Boards located on the sample transfer mechanism.

4A6.2 Analytical Electrode Assembly

The Analytical Electrode Assembly contains the ion selective electrodes that perform quantitative measurements of sodium, potassium, and carbon dioxide. The electrode assembly is mounted on the TECHNICON RA-XT system. It consists of the Na^+, K^+ and CO_2 ion selective electrodes, and a silver/silver chloride reference electrode. The output wire from each electrode is connected to the ISE Amplifier Board behind the electrode assembly.

A transparent electro-static cover shields the electrode assembly. The cover improves electrical isolation of the ion selective electrodes signals which can be affected by electrical noise. A delay loop contained in a water bottle is located on the front panel under the electrode assembly. The delay loop is used to make the sample arrive at the Analytical Electrode Assembly at the proper time, and to stabilize the temperature of each sample.

The electrode assembly requires periodic cleaning to maintain proper operation. In addition to cleaning, the potassium and carbon dioxide electrodes also require periodic replacement of their respective membranes, and replenishment of the KCI solution in their electrode caps. The sodium electrode requires daily etching of its glass membrane in order to provide proper sensitivity.

Figure 4AFO1 ISE MODULE INTERFACED WITH RA-XT SYSTEM

4B DETAILED FUNCTIONAL DESCRIPTIONS

This section provides detailed theory of operation for each system function. The functions are as follows: Analytical Electrode Assembly operation, signal processing and A/D conversion, air injection and sample and reagent delivery, ISE Display Panel, ISE Sample Probe Transfer Mechanism operation, RA-XT/ISE Module interface, ISE CPU Control Board operation, and power distribution.

4B1 Analytical Electrode Assembly

The TECHNICON RA-XT system utilizes ion selective electrodes to determine the concentrations of sodium (Na^+), potassium (K^+), and carbon dioxide (CO_2) in serum or urine samples. In its simplest form, the measuring device is an electro-chemical cell consisting of: ion selective electrodes, the solution under test, and the reference electrode. The potential of an ISE is measured with respect to the reference electrode, as shown in Figure 4B-1.

Figure 4B-1 SIMPLIFIED DIAGRAM OF ISE MEASURING SYSTEM

4B1.1 Electrode Selectivity

The Na+ electrode has a glass membrane highly selective to the Na+ ion. The K+ electrode utilizes an exchange valinomycin membrane highly selective to potassium ions. The CO_2 electrode is similar to the K+ electrode, but the membrane is a carbonate ionophore pcv matrix selective to carbonate. As shown in the electrode diagrams (Figures 4B-2, 4B-3, and 4B-4), a KCI solution is in contact with a reference electrode, a silver/silver chloride wire. The KCI solution contains the ions being measured, but at a constant concentration. The sample and reference streams flow in opposite directions, and meet to form a liquid junction that permits electrical contact between ISEs (Figure 4B-5).

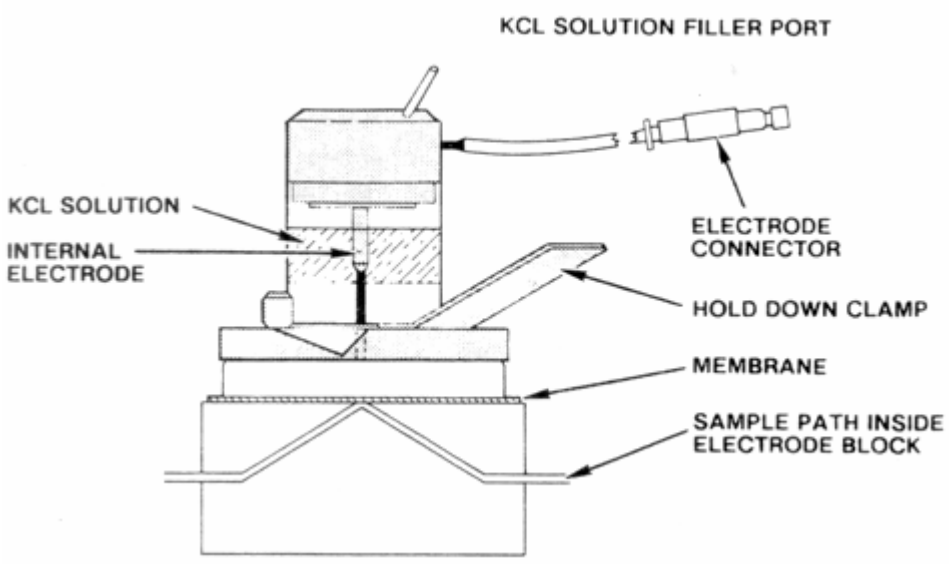


Figure 4B-2 CO_2 AND K ELECTRODE ASSEMBLIES

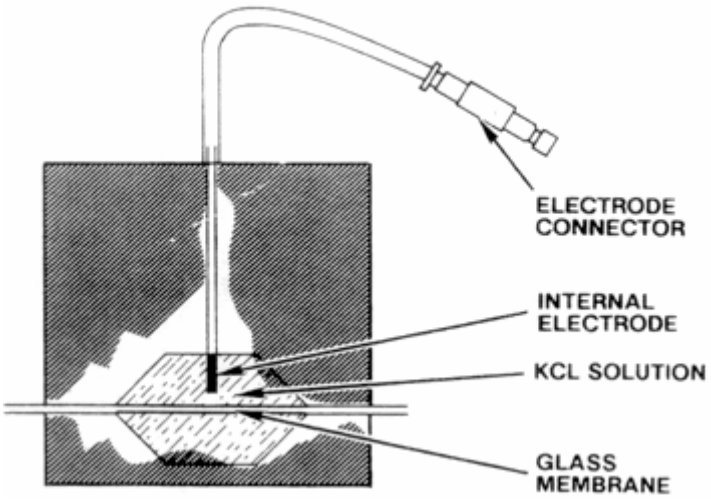


Figure 4B-3 Na ELECTRODE ASSEMBLY

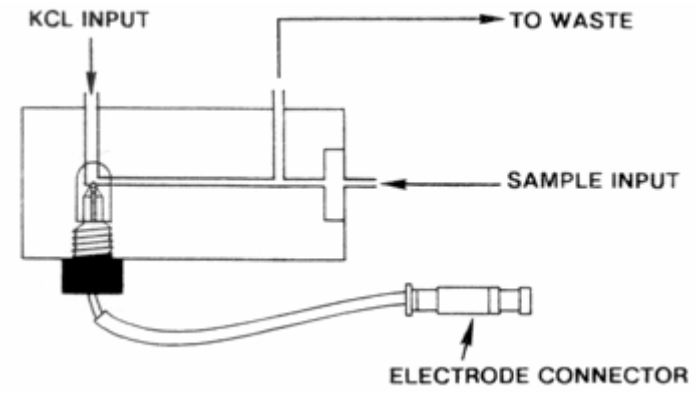


Figure 4B-4 REFERENCE ELECTRODE ASSEMBLY

The Na+ electrode has approximately a 300:1 selectivity for sodium over potassium when freshly washed out. The K+ electrode has a selectivity of 4000:1 for potassium over sodium. The electrical output from each ISE is compared with the output of the silver/silver chloride reference electrode.

The electrical signals produced by each ISE are small enough to be affected by electrical noise. The transparent cover of the assembly is an electrostatic shield, which improves electrical isolation. A ground wire situated in the analytical stream prevents noise generated in the stream from feeding back into the Analytical Electrode Assembly. The sample and counterflow streams must flow continuously, otherwise depletion will occur where the KCI and sample stream meet.

Figure 4B-5 ISE ANALYTICAL MODULE

The buffered serum or urine sample is segmented with air bubbles as it is pumped to the Analytical Electrode Assembly. As the buffered sample flows past the ISE membranes, the concentrations of Na^+, K^+, and CO_2 in the sample cause changes in the electrical potential that exists between the ionically variable outer surface and the ionically constant inner surface of each ISE. These changes in electrical potential are automatically compared with the common reference electrode. The resulting difference signals between the measuring electrode and the reference electrode are amplified on the ISE Amplifier Board to acceptable levels for use by the A/D Converter Board. During standby periods, wash solution is continuously in contact with the ISEs to ensure high stability and rapid response.

4B2 Two-point Calibration

Calibration of the ISE module must be performed daily before samples are analyzed for Na^+, K^+, and CO_2 concentration levels. Also, a calibration is required following a clean/etch operation or whenever the sample mode (serum or urine) operation is changed. Low and high calibrators are used to establish the slope. Since the range of a urine sample is greater than the range of a serum sample, a separate Hi Cal calibrator is required to determine the urine sample slope. A range or drift error that occurs during normal operation will inhibit further processing of ISE tests until a new two-point calibration is established.

At the start of a two-point calibration, the ISE probe makes six aspirations from the wash receptacle. The readings from the repetitive wash samples are used to standardize the system, to ensure that amplifier range limits are not exceeded, and to establish a baseline value.

The first wash reading is used to establish a reference set point of approximately 5 volts. This voltage is the standard against which unknowns are subsequently compared. The set point voltage is produced when an AMP ADJUST signal is issued from the ISE CPU Control Board as the first wash readings are taken.

The second wash reading is used to check that the Amp Adjust values are within ?2 volts of the set point obtained from the first wash. If it is not within this limit, an AMP ADJUST error is printed out for the second wash reading.

The third and fourth wash readings are ignored by the software unless the A/D counts exceed the voltage range of the amplifier, in which case a RANGE ERROR is flagged for the errant channel. The amplifier limits are set at 1 to 9 volts.

The fifth and sixth wash readings are stored, and used to check for drift. Eleven readings are stored for each wash. The mean difference between wash 5 and wash 6 is compared with a stored limit. If the mean difference does not exceed this limit (15 A/D counts) the readings for wash 5 and 6 are averaged. This average is then used to perform a baseline adjust (single-point calibration). If the mean difference between wash 5 and wash 6 exceeds the stored limit, a DRIFT ERROR is displayed.

After the six wash aspirations, the ISE sample probe sequentially aspirates three buffered Lo Cal samples and three buffered Hi Cal samples from the reaction cuvettes. The results of the first Lo Cal sample and the first Hi Cal sample are discarded. The results from both the second and third Lo Cal and Hi Cal samples are used to calculate the Nernst slope. The accepted slope must be in the range of 45 to 65 mV per decade for Na+ and K+, and 19 to 30 mV per decade for carbon dioxide. An example of how the slope is calculated follows.

Example:

Channel = Sodium

Amplifier Gain = 25

Analog to Digital Conversion Factor = 1.68

Slope = (log Lo Cal/Hi Cal)($A/D_{Hi\ Cal}$ - $A/D_{LO\ Cal}$)

LO CAL =115 mmol/L (average of A/D counts = 9657)

HI CAL = 170 mmol/L (average of A/D counts = 9272)

Na^+ Slope = (log 115/170) (9657-9272) = 2268 A/D counts

Conversion of A/D to mV = 2268/1.68 = 1350 mV (after amp)

Slope in mV @ Electrode = 1350/25 = 54 mV

Table 4-2 SLOPE LIMITS

ISE	IDEAL	ACCEPTABLE
Na	59.6	45-65
K	59.6	45-65
CO_2	29.8	19-30

4B3 Signal Processing and Data Acquisition

This section describes the components that condition the analog signals from the electrodes, and convert them to a form that is usable by the CPU.

4B3.1 ISE Amplifier Board

The ISE Amplifier Board contains the signal processing circuits for the Na+, K+, and CO_2 electrodes (see Figure 4B-6). The ion selective electrodes respond to their respective ion concentrations according to the Nernst equation. The samples for ISE analysis are appropriately buffered to provide a medium of constant ionic strength. Then the Analytical Electrode Assembly can be calibrated to measure ion concentration rather than activity. The gain and analog output voltage ranges (see Table 4-3) of each ISE amplifier circuit are designed to meet the operating requirements of the A/D converter stage, which follows the ISE amplifiers.

Figure 4B-6 SIMPLIFIED DIAGRAM OF ISE AMPLIFIER CIRCUIT

Listed in Table 4-3 are expected voltage levels and A/D counts for the ISE module.

TABLE 4-3 ISE AMPLIFIER PARAMETERS

AMPLIFIER SETTINGS	SODIUM	POTASSIUM	CARBON DIOXIDE
AMP ADJUST SET POINT (Approximate middle of A/D range.)			
VOLTS	5.4	4.28	4.28
A/D COUNTS	9000	7135	7135
GAIN (Low)	25	30	30
AMP ADJUST DRIFT LIMITS			
VOLTS	?2	?2	?2
A/D COUNTS	?3333	?3333	+ 3333
(Low to High)	(5667 to 12333)	(3802 to 10468)	(3802 to 10468)
AMP RANGE LIMITS			
LOW LIMIT: VOLTS	1.0	1.0	1.0
A/D COUNTS	1666	1666	1666
HIGH LIMIT: VOLTS	8.9	8.9	8.9
A/D COUNTS	15000	15000	15000

4B3.2 Preamp Circuits (Refer to Figure 4BFO1 and Schematic 108-C463.)

The Na+, K+, and CO_2 amplifier circuits are basically alike, but the overall gain and offset voltages are specific to each channel. The overall gain of the Na^+ channel is 25. The K^+ and CO_2 channels each have a gain of 30. The following description of the K^+ channel also applies to the Na^+ and CO_2 channels.

The analog signals from the K^+ electrode and the reference electrode are applied to non-inverting buffer amplifiers U4 and U2, respectively. The differential between the two signals is amplified by a factor of 6.3 by amplifier U6. The output of U6 is fed to the low pass filter stage U9 where the signal is amplified by a factor of 2. The signal is filtered by U9 to eliminate any noise or disturbances (developed by the electrode) from interfering with the signal being measured. The filtered signal is summed with the offset voltage developed by the amplifier adjust circuit, and then amplified by a factor of 2 by amplifier U18. The analog signal is output through J6 to the A/D Converter Board where it is converted to a digital signal proportional to the analog level.

Each circuit is designed to meet the requirements of the following formula, which is derived from the Nernst equation:

V_0 electrode = (constant) (total gain) (log Δ concentration)

4B3.3 Amp Adjust Circuit

Electrode voltage stability is accomplished by the amp adjust circuit, which is incorporated into the preamp circuitry to ensure the accuracy of the output data. The signal received by the V/F Converter Board is defined as: V_o *electrode + offset voltage = measured potential.* The preamps for the Na+, K+, and CO_2 tests are adjusted to the set point or mid-range of the A/D converter stage during a single-point calibration. The single-point calibration measures the concentration of the low cal calibrator present in the wash solution. The A/D ranges and set points for the respective tests are as follows:

- *Sodium* - 2.2 to 8.0 volts, set point 5.4 volts at a concentration of 130 mEq/L
- *Potassium* - 1 7 to 8.2 volts, set point 4.28 volts at a concentration of 10 mEq/L
- *Carbon Dioxide* - 1 9 to 6.8 volts at a concentration of 15 mEq/L

If the amp adjust circuit fails to bring the signal into the working range of the A/D circuitry, an alert is printed out indicating a range or drift error.

The amp adjust circuit for each channel functions the same way; however, the comparator threshold voltage is specific for each channel. The amp adjust circuit operates in the following manner: On the rising edge of the amp adjust signal, opto isolator U7 turns on. NAND gate U15-3 goes to a logic 0 and clears counters U26 and U27. D flip-flop U16 is preset to a logic 1 on the Q output. On the falling edge of the amp adjust signal, U7 is turned off. Counters U26 and U27 are enabled as U15-3 goes to logic 1. NE555 timer U10 is enabled and issues clock pulses to counters U26 and U27 through NAND gate U15-6. As the counter output increases, the output of D/A converter U21 is driven toward-10 volts. As the output of U21 pin 4 becomes more negative, the output of summing amplifier U18 becomes more positive.

The output of U18 is input to comparator U28. As the output of U18 approaches the comparator threshold voltage, a pulse is issued from the comparator that clocks D flip-flop U16. The Q output of U16 then goes to a logic 0, and inhibits the clock pulses to counters U26 and U27. The Q output of U16 goes to a logic 1 and is input to NAND gate U14. (All inputs to U14 must go to a logic 1 before latch U12 is reset and inhibits clock pulses from U10.)

4B3.4 A/D Converter Board (Refer to Figure 4BFO2 and Schematic 108-C437.)

The A/D Converter Board transforms the Na+, K+, and CO_2 analog voltages into proportional digital levels. It is mounted on the ISE Data Acquisition Board.

4B3.4.1 Circuit Description

The electrode voltages from the ISE Amplifier Board are input to multiplexer U1 through coaxial cables. The shield on each cable is terminated on the ISE Amplifier Board to minimize noise effects.

During a read period, logic level control signals are output from PIA U9 on the Data Acquisition Board to multiplexer U1 on the A/D Converter Board. The control signals cause the respective analog switches, internal to U1, to close sequentially for 16.5 ms each. The control signals are input to pins 1 and 16 of multiplexer U1.

The truth table for these control functions is given in Table 4-4.

Table 4-4 ISE INPUT CONTROL

U1-16	U1-1	SELECTION
0	1	K+
0	0	Na+
1	0	CO_2

The respective analog voltages and the ground reference are switched through U1, and input to amplifier AR1, which has a gain of 1.19. The amplified output is input to Voltage-to-Frequency (V/F) Converter U2 for a period of 16.67 ms. The V/F converter changes the d-c analog voltage into a digital pulse train equivalent to the analog level (the higher the voltage, the higher the frequency). The signal is buffered by U3 before exiting the board through E11. The V/F converter is capable of reading analog input voltages form 0 to 10V d-c. A 10-volt input signal is converted to an output frequency of 1 MHz. The input voltages are scaled to about 100 kHz/volt.

Amplifier AR1 may be nulled by placing jumper P1 between E18 and E19 (GND), jumper P2 between E21 and E22 (GND), and then adjusting R7 so that the voltage between TP1 and TP2 is 0 V dc.

NOTE

To avoid damage to multiplexer U1, disconnect J1, J2, and J3 when nulling amplifier AR1.

4B3.5 Data Acquisition Board (Refer to Figure 4BFO2.)

The Data Acquisition Board performs two functions: a) it provides the commands to control the multiplexing of the K^+, Na^+, and CO_2 analog signals through the A/D Converter Board; b) it retains the counts for the respective analytical tests in digital form until called for by the system microprocessor.

The A/D Converter and two programmable peripheral devices are mounted on the board. The peripheral devices are Peripheral Interface Adaptor (PIA) U9 and Programmable Interval Timer (PIT) U8. The microprocessor communicates with the Data Acquisition Board through PIA U9 and PIT U8. The PIA consists of a data bus buffer, read write control logic, and three ports. A control word from the microprocessor sets up the ports in one of three modes of operation: for PIA U9, port A is an output; port B is an input; and port C is not used.

PIT U8 consists of a data bus buffer, read write control inputs, command register, and three independent 16-bit down counters (0, 1, and 2). Counter 0 is used to accumulate the 0- to 1-MHz K+ and CO_2 transitions from the A/D Converter Board. The counts for each test are loaded into counter 0 for one period of the power line frequency (16.67 ms for 60-Hz systems or, 20-ms for 50-Hz systems). Counter 1 accumulates the transitions of the 0- to 1-MHz Na^+ signal from the A/D Converter for one period of the power line frequency. Counter 2 acts as a time base counter driven by a 1-MHz frequency to produce either the 16.67-ms count gate for 60-Hz systems or the 20-ms count gate for 50-Hz systems. The input to U8 pin 16 (gate 2) is high for 16.67 ms or 20 ms. The carry output from counter 2 is issued from U8 pin 17. It establishes the gating periods for counter 0 and counter 1. The accumulator counts are scaled in the following manner:

- Domestic systems = 1965 counts/volts.
- International systems = 2322 counts/volt.

The main microprocessor program selects either PIA U9 or PIT U8 by supplying the address number for either U9 or U8 to PROM U3 on the Data Acquisition Board. PROM U3 issues the chip select signals that enable each device.

4B3.5.1 Circuit Description (Refer to Figure 4B-7 and Schematic 108-C433.)

The A/D Converter changes the Na^+, K^+, and CO_2 electrode voltages into digital pulses, which are proportional to the respective analog voltages. The digital signals are sequentially input to PIT U8 on the Data Acquisition Board. The read time commands are output to the A/D converter from U9 ports PA6 and PA7.

While the sample is in the Analytical Electrode Assembly, readings are taken every half second for a period of about five seconds. A total of eleven readings are taken to allow each electrode to stabilize at the proper signal level. To process the respective electrode data the following conditions are present on the Data Acquisition Board:

1. Counter 0 and Counter 1 (internal to U8) are loaded with 1's by the system microprocessor prior to each read period.

2. When the system is powered on, the logic 0 reset pulse causes the output of NAND gate U4-6 to go to a logic 0 and clear D flip-flop U2. The -Q output from U2 is then set to a logic 1.
3. The time base counter (Counter 2) is loaded with 1's at system startup. The number in the counter is equivalent to either 16.67 ms or 20 ms.
4. Counter 2 is clocked at a 1-MHz rate. The clock pulses are loaded into the counter through pin 16, the Gate 2 input on IC U8.
5. When Gate 0 goes to a logic 1, Counter 0 is clocked down to the equivalent K^+ value by the digital pulses from the A/D Converter Board. The clock pulses enter the counter through the Clock 0 input on U8. Gate 0 is produced when the inputs and NAND gate U4-8 go to a logic 1. Concurrent with Gate 0 going to a logic 1, Gate 2 is brought to a logic 1 at the output of OR gate U5-6. Gate 2 enables Counter 2 to be clocked by the 1MHz input to clock 2 of U8.
6. Gate 0 and Gate 2 remain at a logic 1 for 16.67 ms as established by the time base counter. At the completion of the 16.67-ms period, D flip-flop U2 is clocked by U8 pin 17, changing Q to a logic 1 and the -Q to a logic 0.
7. A logic 0 from port PA2 makes the output of NAND gate U4 go to a logic 0 and clear D flip-flop U2 to a logic 1 on the -Q output.
8. When Gate 1 goes to a logic 1, Counter 1 starts clocking down to the equivalent Na+ value synchronously with the digital pulses from the A/D Converter Board. Gate 2 is again brought to a logic 1 to enable the clocking of Counter 2 for 16.67 ms.
9. During the third 16.67-ms period, CO_2 data is clocked into Counter 0 by the digital pulses from the A/D Converter Board.
10. Counters 0 and 1 repeat the process described above eleven times during each five-second read period.
11. At the completion of the read time, port PB0 on U9 remains at a logic 0, informing the microprocessor that the read time has been completed.

Figure 4B-7 DATA PROCESSING TIMING DIAGRAM

4B4 Air Injection (Refer to Figure 4BFO3.)

In order to reduce carryover between samples, air bubbles are injected into the diluted sample stream as it is aspirated from the reaction tray cuvette. The air injection circuit is used also to clear out the ISE sample probe as it leaves the wash receptacle.

Each bubble is a slug of 5-psi air that gets trapped between pinch valves 3 and 4. Pinch valve 3 opens first for 20 ms, then closes to trap the air. After a 50-ms delay, pinch valve 4 opens for 20 ms to release the trapped air into the ISE sample probe. The pressurized air comes from the air pump located at the rear of the TECHNICON RA-XT system.

The commands to pinch valves 3 and 4 are generated on the ISE CPU Control Board. The circuit consists of programmable I/O port U29 (8155A) and line drivers internal to IC U27. Troubleshooting LEDs DS11 and DS12 are connected to the driver output lines. The LEDs illuminate as the air bar command lines go to logic 0. During the air injection period, logic 1 pulses (20 ms in duration) are issued from J4 on the ISE CPU Control Board through pins 3 and 5. The pulses are coupled to pinch valve circuits 3 and 4 on the Air Injection Control Board. The pinch valve circuits on the control board are identical. When a logic 1 pulse is input to either circuit, the solenoid becomes energized. This pulls the pinch bar down, and allows the air to pass through the tubing.

4B4.1 Air Injection Control Board (Refer to Schematic 108-C104.)

The Air Injection Control Board controls the operation of air inject pinch valve solenoids 3 and 4. A logic high air inject command from the ISE CPU Control Board turns on the LED internal to IC U1. The detector output of U1 then goes low as light from the LED strikes it. The low is inverted by U2 to a high, and turns on NPN transistor Q1 Current then flows through the solenoid to ground, which pulls down the pinch bar.

When the air inject command goes low, transistor Q1 turns off. With the transistor off, the pinch valve solenoid is de-energized, which allows the pinch bar to lift and compress the air tube.

4B5 Sample and Reagent Delivery

The reagent pump located on the ISE Pump/Electronics Module is driven by a stepper motor. The stepper motor is controlled by the 8741A I/O CPU on the ISE CPU Control Board. The commands from the 8085 microprocessor on the ISE CPU Control Board instruct the 8741A to take control and generate the logic level motor drive signals.

The reagent pump stepper motor is actuated twice during each 15-second analytical cycle. During this period, the following operations occur.

1. The ISE probe travels from the wash receptacle to the reaction cuvette. The reagent pump first actuates about one second after the ISE probe enters the reaction cuvette. It remains on for about three seconds.
2. During the three-second period, the contents of the Analytical Electrode Assembly are pumped to waste, the ISE air injectors energize and inject seven air bubbles into the sample stream; the diluted sample is aspirated from the reaction cuvette into the delay coil; counterflow reference solution is pumped to the reference electrode compartment in the Analytical Electrode Assembly; and cal/wash solution is pumped to the wash receptacle.
3. The reagent pump then shuts off for about two seconds as the probe travels back to the wash receptacle.
4. The reagent pump actuates a second time for about two seconds and pumps cal/wash solution into the delay coil. It replenishes the wash receptacle and pumps any overflow from the wash receptacle to waste.

4B5.1 Circuit Description (Refer to Figure 4BFO4.)

Figure 4BFO4 is a functional block diagram showing how the reagent pump stepper motor is controlled. Motor operation is initiated by the ISE microprocessor commands sent to the 8741A CPU. The 8741A's internal program sets the stepping rates and the period of actuation of the motor while the probe is in the reaction cuvette, and again when the probe is in the wash cup. During the aspirate and wash cycles, the motor ramps up 50 steps per second to the constant speed of 543 steps per second. The motor is on for three seconds during the aspirate period and two seconds during the wash cycle.

When the commands are received by the 8741A, the appropriate stepper motor control signals are generated. The 8741A produces four stepper motor control signals: ϕ1, ϕ2, ϕ3, and ϕ4. These signals are buffered and sent to the Stepper Motor Sensor Board where they are transformed into the drive level signals required by the motor. Drive level voltages are supplied to the stepper windings by the ISE Heat Sink Assembly.

4B5.1.1 8741A CPU

When the 8741A is selected, the internal 8741A program takes control. The 8741A communicates with the main microprocessor through an internal data bus buffer, I/O register, and an 8-bit data bus buffer status register with four bits user definable. The status bits are as follows:

F1 = 1	Main microprocessor requests status.
F1 = 0	Main microprocessor requests or transmits data.
F0 = 1	Stepper motor is in motion.
F0 = 0	Stepper motor has stopped.
IBF	(Input Buffer Full)
IBF = 1	Main microprocessor has sent data or an instruction to be acted upon.
OBF	(Output Buffer Full)
OBF = 1	Error flag indicating that the data received from the main microprocessor cannot be processed successfully.

As dictated by the 8741A internal program, the data words for the stepper motor phases are issued through I/O port 2. The active high phase command from the 8741A is sent to the NAND gate portion of power ICs U30 and U31 (75461's). The low output of the gate turns off the transistor portion of the IC, driving the collector high to produce the ϕ1, ϕ2, ϕ3, and ϕ4 logic level command signals. The commands are then presented to the Sensor Control Board. LEDs DS1 through DS4 are connected to the output lines of U30 and U31. The LEDs illuminate when the output commands are present.

4B5.1.2 Stepper Motor Sensor Board (Refer to Schematic 108-C097.)

The Stepper Motor Sensor Board controls the turning on and off of motor drive currents by means of four transistor switches. The transistor switches are operated by the ϕ1 through ϕ4 logic level command signals from the ISE CPU Control Board. 24 V dc is supplied to transistors Q1 through Q4, and to voltage regulator VR1. The voltage regulator provides a +5-V d-c output to opto-isolators U2 and U1, and to inverter U3. The + 5 V dc supplied to these devices is isolated to eliminate any noise interference that might be picked up from the motor circuit.

Diodes CR1 through CR8 are used to suppress any voltage spikes over 24 volts, which might result from the inductance of the motor.

4B6 ISE Display Board (Refer to Figure 4BFO5.)

The ISE Display Board is used to display messages from the ISE Pump/Electronics Module and from the RA-XT system through a 4-digit LED module. The board also indicates the STARTUP, READY, and OPERATE states of the ISE module by illuminating one of three incandescent lamps on the board.

The display board is controlled by the 8085A microprocessor on the ISE CPU Control Board. The 8085A communicates with the display module and state indicator lamps through two IC interface devices. Commands to the LED display are output through ports A and B of U15, an 8255A PIA. Commands to the state indicator lamps are output through port A of U29, an 8155 combination RAM and I/O device.

4B6.1 Circuit Description (Refer to Schematic 108-C452.)

The LED display consists of 4-digit modules, which illuminate to form alpha-numeric characters. Sixty-four ASCII characters can be displayed, as shown in Figure 4B-8. The display IC contains memory, a ROM decoder, multiplexing circuitry, and drivers. The LED display module is selected when a logic 1 RW1 signal is output from PA2 of PIA U15. The signal is inverted by U12 to a logic 0, and input to pin 9 of DS4.

Figure 4B-8 ASCII DISPLAY CHARACTERS

A digit is selected on the LED module by the logic 1 and 0 pattern output from U15 ports PA0 and PA1, as shown in Table 1 of Figure 4BFO5. The data to illuminate each of the alphanumeric characters are issued from ports PB0-PB6 of U15. The data are buffered through line driver U14, and input to pins 16 through 22 on LED display module DS4. The module is cleared through pin 5 when the system is reset.

The state indicators are 5-V d-c incandescent lamps, which correspond to the three operating states. The STARTUP lamp illuminates when any one of the following conditions occurs:

1. Power is applied to the Pump/Electronics module.
2. The reset button on the ISE Control/Driver PCB or RA-XT system is pressed.
3. Program operation reverts to the start-up state.

The READY lamp illuminates when all the acceptable operating conditions are met. In this state, the ISE hardware is held in a state of readiness for commands from the RA-XT system. The commands may be a request to go to the operate mode and/or a diagnostic routine.

The OPERATE lamp illuminates when a SAMPLE command from the RA-XT system is sent to the ISE CPU Control Board. The ISE CPU initiates and controls the process for the Na^+ /K^+ /CO_2 analyses.

The three state lamps - DS1, DS2, and DS3 - are controlled by logic level signals from PA0, PA1, and PA2 of RAM I/O U29. The signal to illuminate a lamp comes from U29 as logic 1. The signal is inverted be U1 on the display board, and then applied to the lamp. The lamps are powered by 5 V dc.

4B7 ISE Sample Transfer Mechanism (Refer to Figure 4BFO6.)

The sample probe transfer mechanism for RA-XT systems with the ISE option includes an ISE resample probe transfer assembly. Vertical motion is imparted to the sample and ISE resample probes simultaneously by a common rotational axis and drive motor. Horizontal motion, however, occurs independently.

The SWING MOTOR ON and PROBE ARM position commands from the ISE microprocessor are output through port A of U15 (an 8255 PIA) to associated logic chips. Sensor signals from the wash cup, reaction cuvette, and etch/clean stations on the transfer mechanism inform the microprocessor of the position of the ISE probe. The signals are input to port C of PIA U15. A MOTOR ENABLE command is output from RAM I/O U29, and is issued to associated logic control chips on the control board. The MOTOR ENABLE command occurs only when the system is powered on.

The ISE resample probe's horizontal motion is controlled by commands from the ISE CPU Control Board to the DC Motor & Sensor Control Board. The DC Motor & Sensor Control Board converts the logic level commands to d-c drive currents for the 24-V d-c horizontal motor. The SWING MOTOR ON command is monitored by LED DS6. The reaction tray, wash cup, and etch/clean sensor signals are monitored by LEDs DS9, DS8, and DS7, respectively.

The ISE resample probe can be driven to any one of three positions: wash cup, reaction cuvette, or etch/clean station. To actuate the ISE resample probe swing motor, PIA U15 outputs a logic 1 from PA3. A probe position code is issued also from PA5, PA6, and PA7 of port A to comparator U3. A logic 0, programmed into one bit of the probe position code, denotes the probe destination.

The logic 1 output from port PA3 presets D flip-flop U1. The Q output of U1 then goes to logic 1, and actuates the probe SWING MOTOR ON command. The command is issued from pin 17 of the ISE CPU Control Board, and is presented to the DC Motor & Sensor Control Board. Switch S1 on the DC Motor & Sensor Control Board then closes, and directs 24 V dc to the horizontal motor.

Comparator U3 on the ISE CPU Control Board monitors the position sensors on the transfer mechanism. When there is a match between the position code sent by the sensors, and the position code previously loaded into U3, the motor is turned off.

4B8 RA-XT System/ISE Module Interface (Refer to Figure 4B-9.)

The RA-XT system CPU and the ISE CPU communicate through an RS-232 interface in a master/slave relationship. Communication occurs at 600 baud during program download, and at 9600 baud after the ISE program is fully downloaded into the ISE CPU Control Board memory. Programmable Interval Timer U36, located on the ISE CPU Control Board, controls the baud rate. Data transmit and receive functions are performed by USART U17. A second USART (U18) is used for off-line testing.

Line Driver U6 converts TTL level signals to RS-232 level signals. Line Receiver U5 converts RS-232 level signals to TTL signals. The interface cable is connected between 1J2 on the RA-XT system side panal, and 2J1 on the ISE/Electronics Module.

4B8.1 USART Description

USART U17 is configured to operate in the asynchronous mode. The USART converts output data from parallel form to serial form, and converts input data from serial form to parallel form. As a transmitter, it adds start and stop bits to the data words, generates parity, and clocks the data out at the required rate. As a receiver, it recognizes and deletes start and stop bits, checks parity, and clocks the data in at the required rate. It also provides indicators that signal whether it has received data or is ready to accept data for transmission. The indicators may signify errors in the received data also.

Serial data is transmitted between the RA-XT system and the ISE Pump/Electronics Module in the following format: 1 start bit, 8 data bits, 1 parity bit (check for even parity), and 2 stop bits.

When receiving data from the RA-XT system, the DSR (Data Set Ready), CTS (Clear to Send), and RxD (Received Data) signal lines are at the following levels:

- DSR is changed from a high RS-232 level to a logic 0 TTL level by Line Receiver U5.
- CTS is grounded, and therefore held at logic 0.
- RxD serial input data is changed from the RS-232 levels to TTL logic levels by U5.

When transmitting data to the RA-XT system, the Request to Send signal (RTS) is changed from a TTL logic 0 to a high RS-232 level by U6. TxD is a serial data output.

4B9 Program Downloading

The operating programs for the RA-XT system and the ISE Pump/Electronics Module are contained on the same floppy disk. The ISE program is downloaded from the disk to the 16k RAM located on the ISE CPU Control Board.

The downloading operations are controlled by PROM U56 located on the RA-XT system CPU board. The ISE configuration switch also is located on the RA-XT system CPU board. This switch should be set to the OFF (ISE option installed) position when the ISE Pump/Electronics Module is interfaced to the RA-XT system.

A bootstrap program resident in PROM U22, located on the ISE CPU Control Board, loads the ISE program into the 16k RAM memory on the ISE CPU Control Board.

4B9.1 Downloading Messages

The message **LDOK** appears on the ISE display panel when the ISE program is successfully downloaded to the ISE CPU Control Board. If downloading is unsuccessful, the message **NLOD** is displayed. The following protocol is used to download the program:

1. When power is applied to the RA-XT system, and the program disk is loaded, the RA-XT system sends a character to the ISE CPU Control Board to initiate downloading of the ISE program.
2. The RA-XT system CPU then waits for a character from the ISE CPU indicating the start of the download protocol.
3. If the program is loaded without any problems, the RA-XT system CPU waits for an acknowledgement character. The message **LDOK** is then displayed.
4. If the character at the start of the protocol does not arrive at the RA-XT system CPU within a specified period of time, the RA-XT system CPU sends another character to the ISE CPU. If the ISE CPU does not respond with a compliment of that character within approximately 80 milliseconds, one of the following error messages appears on the ISE display. **TRBE** (transmission bit error), **TRTE** (transmission timing error), **BCER** (byte counter error), or **CHKE** (checksum error). The software then makes five attempts to download the program, each time checking for the start-of-protocol character. If the program fails to load, the ISE CPU sends a character back to the RA-XT system CPU and the message **NO LOAD** appears on the RA-XT system display module, and **NLOD** appears

on the ISE Pump/Electronics Module display.

5. If the program successfully loads to the point of comparing checksums, and then fails, the software will make five more attempts to download. If the program still fails to load, a character is sent to the RA-XT system CPU and the message **NLOD** appears on the ISE display, and **NO LOAD** appears on the RA-XT system display module.

4B10 RA-XT System Software Control of ISE Functions

The RA-XT system performs the following ISE functions:

- Downloads the ISE operating program
- Monitors the baseline readings for drift
- Corrects the readings for drift
- Computes the ISE concentration levels
- Flags sample results that are outside the accepted ranges
- Provides SAMPLE commands to the ISE Pump/Electronics Module every 15 seconds
- Keeps track of the time of the last ISE calibration
- Performs automatic phasing of the ISE Pump/Electronics Module when requested by the operator
- Performs periodic etching requirements
- Recognizes reagent tray position 13 as the duluting buffer
- Provides diagnostic routines to check ISE hardware operation

4B11 ISE Pump/Electronics Module Operational States (Refer to Figure 4B-11.)

The ISE Pump/Electronics Module sequences through three operational states before executing any commands to process samples. The states are: STARTUP, READY, and OPERATE. The states are displayed on the ISE Pump/Electronics Module front panel.

STARTUP STATE

The ISE CPU enters the STARTUP state when power is applied to the module, when the RESET button the ISE CPU Control Board is pressed, or when the program returns the ISE CPU to this state. In the STARTUP state, a series of diagnostic checks are automatically performed before the ISE operating program is downloaded by the RA-XT system CPU. When all conditions have been met, the ISE CPU places the ISE module in the READY state.

READY STATE

In the READY state, the ISE CPU waits for commands from the RA-XT system CPU. The commands direct the ISE CPU to enter the OPERATE state, or to perform a diagnostic routine. A periodic cleaning protocol is initiated automatically in this state also.

OPERATE STATE

When the system ISE Pump/Electronics Module enters the OPERATE state, the software scans the worklist for ISE selections. If an ISE test was requested, and a valid two point calibration is in effect, the ISE module initiates the OPERATE state functions when it receives a SAMPLE command from the RA-XT system.

Figure 4B-9 OPERATIONAL STATE FLOWCHART

4B12 ISE CPU Functions (Refer to Schematic 108-C410.)

The ISE CPU Control Board is the data communication link with the RA-XT system CPU. The board also executes the ISE operating program for the following functions:

- Stepper motor control of the peripump
- Swing motor control of the ISE probe
- Actuation of ISE air valves V3 and V4
- Status lamp illumination
- ISE alphanumeric display
- Front end ISE amplifier adjust control
- Control of the A/D functions
- ISE sample processing and data transmission to the RA-XT system

The ISE CPU Control Board contains the following circuits: CPU, memory, serial I/O, and IN/OUT devices.

CPU - An 8085A microprocessor and support circuitry consisting of: ROM U20 (74S472) used for port assignment; decoders U21 and U35 (two 74151担); and octal latch U37 (74LS373). Decoder U21 is used to enable the I/O section while decoder U35 is used to enable the memory section of the control board. The octal latch is required to clock the low order address bits during Address Latch Enable (ALE).

MEMORY - Consists of: 4k of bootstrap ROM on 1C U22 (2732); 16k of RAM (eight 2016担); and 2k RAM chips (U23-U25 and U38-U42). The last page of memory resides in U29 (an 8155-2 combination RAM and I/O IC).

SERIAL I/O - There are two serial receiver/transmitters: U17 and U18 (8251's). U17 communicates with the RA-XT system CPU. U18 is used for off-line testing. A programmable timer, U36 (8253) is used to set up the interrupt rate internal to the ISE unit as well as set the baud rates for the two serial ports.

IN/OUT DEVICES - The I/O circuitry consists of two programmable peripheral I/O ports: U29 (8155A) and U15 (8255A). These two devices are used to control the ISE front panel, ISE probe swing arm controller, front end analog calibration, and two additional air solenoids located in the RA-XT system. An 8741A microcomputer, U16, is dedicated to controlling the reagent pump stepper motor sequences. Bus drivers U9, U10, and U11 are required to communicate with the data acquisition board. Comparator U3 (74LS85) and a flip-flop are used to sense the correct position of the ISE swing arm.

4B12.1 Detailed Description

BUS CONTROL - The 8085A employs a multiplexed data/address bus structure where the address bus conveys the upper eight bits (A8-A15) of a memory or device address only. The data bus (AD0-AD7) conveys both data and the lower eight bits of the address. Demultiplexing is accomplished when the Address Latch Enable (ALE) signal from the 8085A is input to octal latch U37. The AD0 through AD7 bus lines become the lower eight bits of the address when ALE goes to logic 0. Octal latch U37 latches the low order address bits so that a complete address is available to the memory components.

ADDRESS DECODERS - When address lines A8 through A15 are active, ROM U20 outputs a data word to select either an I/O or memory device. I/O or memory addresses are differentiated by the IO/M signal input to U20. The data word from U20 is decoded by address decoders U21 or U35, which produce the chip select signals. Chip select signals for the memory devices are decoded by U21, and chip select signals for the I/O devices are decoded by U35.

RAM MEMORY - The 16k memory consists of eight 2k RAM memory chips. A -WR signal, along with the active chip select signal, will write information into the addressed memory location. A-RD signal, along with the active chip select signal, will read information from the addressed memory location. The last page of RAM memory resides in U29, a RAM memory and I/O device. The 8-bit address, the chip enable input, and IO/-M are all latched by U29 on the falling edge of the ALE signal. The address can be for either the memory section or the I/O section, depending on the level of the IO/-M signal.

Bootstrap PROM U22 is operational when its -RD and chip select lines are active. PROM U22 puts out the instructions required to load the ISE operating program into the 16k RAM memory devices as it is addressed by the 8085A microprocessor.

SERIAL I/O - Two RS-232 serial I/O ports are employed. USARTs U17 and U18. The USARTs are configured for asynchronous operation, and they convert parallel system data into serial data for transmission, or incoming serial data into parallel system data. The USARTs also insert and delete bits or characters as required by the communications format. The USARTs are selected for operation by chip select signals from decoder U35. The C/-D signal, in conjunction with the -WR and -RD input, informs U17 and U18 that the word on the data bus is a data character, a control word, or status information. The -TxC clock controls the rate at which the character is transmitted. The-RxC clock controls the rate at which the character is received. The -TxC and -RxC inputs to U29 are tied together and, therefore, accept the same transmission baud rates from programmable timer U36, pin 13.

PROGRAMMABLE INTERVAL TIMER - The programmable interval timer U36 provides control logic and three counters. Each counter may be programmed to perform a counter or timer function. Programmable timer U36 uses counter 0 and counter 1 outputs. Counter 0 generates the baud rate clock pulses to USARTs U17 and U18. Counter 1 provides the interrupt rate interval to the 8085A CPU. The counters are selected for read or write operation by the A0, A1, -RD, and -WR signals. U36 is selected for I/O operation by the chip select signals from decoder U35.

4B13 Power Distribution (Refer to Schematic 108-C413.)

A-c power for the ISE module is connected to the isolation assembly (P/N 108-B427-01) through a line cord. The isolation assembly can accept a-c input voltages of 100, 120, 220, 234, and 240 volts. The assembly consists of: a voltage selector and fused connector module, power on/off switch S1, shorting switch S2 (located behind a keyplate), isolation transformer T1, a varistor line filter assembly, and terminal block TB1.

4B13.1 A-c Input Voltage Selection

The voltage selector and fused connector module (Figure 4B-10) consists of: a voltate selector PCB, line fuse F1, and a-c the receptacle. The voltage selector PCB has positions to select a-c input voltages of 100, 120, 220, and 240 V ac (shown in Figure 4B-11). The requirement for the 234-V a-c input make it necessary to incorporate shorting switch S2 into the primary of T1 to make it adaptable to the five a-c inputs. The transformer windings are configured to accept the respective a-c input voltages by orienting the voltage selector PCB so that the desired voltage rating is positioned on the top-left side. Switch S2 is set to the closed or open position according to the voltage table in Schematic 108-C413. Shorting switch S2 is situated behind a keyplate to prevent the switch from being set to the incorrect position.

4B13.2 Circuit Description

The a-c circuit shown in schematic 108-C413 is configured for a 120-V a-c input. A 3-amp fuse, located in the voltage selector module, protects the circuit. When power switch S1 is closed, 120 V ac is directed through the switch to the voltage selector PCB. The voltage selector board, in this application, directs the voltage to the proper taps on the primary of transformer T1 for 120-V a-c operation. Switch S2 is closed to limit the 0-125 V winding of T1 to 120 V ac. Movistor RV1 on the primary side of T1 limits peak a-c line transients greater than 275 volts.

The 120 V ac at the secondary of T1 is directed through power line filter FL1, which limits peak noise spikes to 150 V ac. The a-c voltage is output through terminal block TB1 to power supply assembly A3, which consists of + 5 V d-c supply PS3, + 24 V d-c supply PS2, and ?15 V dc supply PS1. The ?5 V d-c supply is protected by CB1, a 0.5-amp circuit breaker. The a-c voltage from TB1 is directed to pump assembly A12 also. +5 V dc and ?5 V dc are supplied to the ISE CPU Control Board and to the Data Acquisition Board. The fan and heat sink assemblies are supplied +24Vdc.

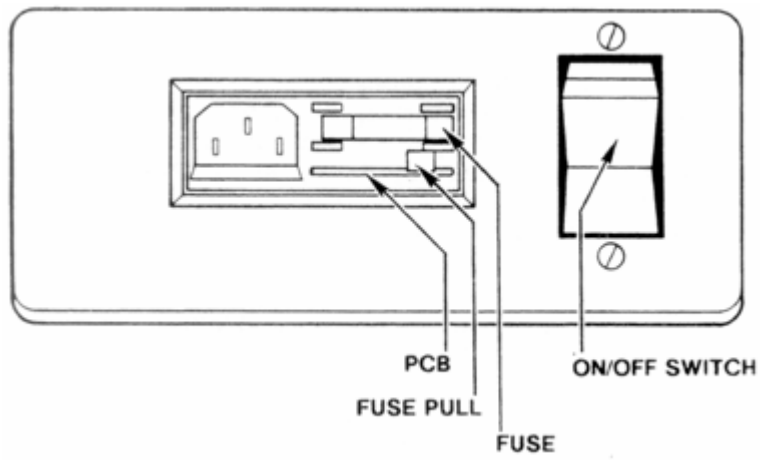


Figure 4B-10 VOLTAGE SELECTOR MODULE

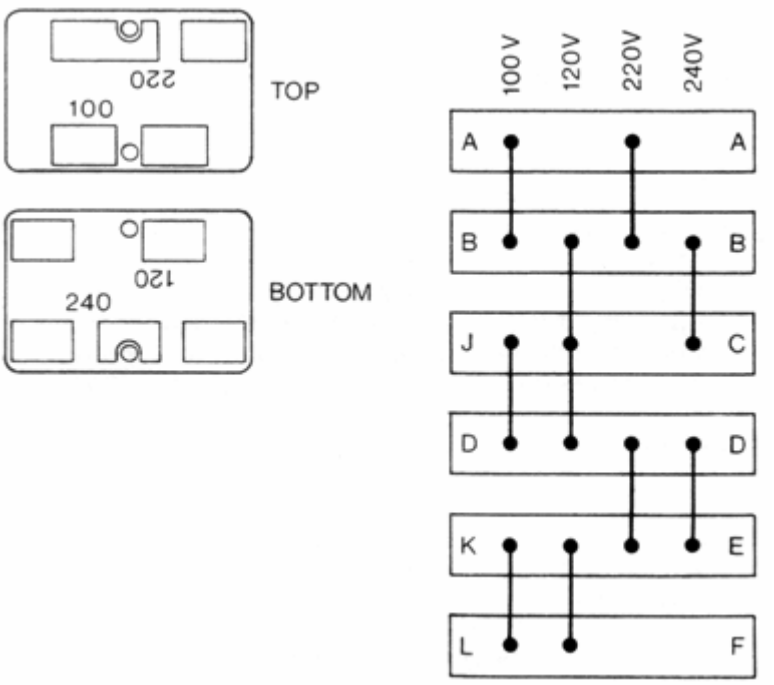


Figure 4B-11 VOLTAGE SELECTOR BOARD AND SCHEMATIC

Figure 4BFO1 ISE ELECTRODE AMPLIFIER CIRCUIT FBD

Figure 4BFO2 A/D CONVERTER CIRCUIT FBD

Figure 4BFO3 PINCH VALVE CONTROL CIRCUIT FBD

Figure 4BFO4 STEPPER MOTOR CIRCUIT FBD

Figure 4BFO5 ISE DISPLAY BOARD FBD

Figure 4BFO6 ISE PROBE TRANSFER MECHANISM CONTROL CIRCUIT

Figure 4BFO7 RA-XT/ISE ELECTRONIC INTERFACE

CHAPTER FIVE

PREVENTIVE MAINTENANCE

WARNING

ONLY QUALIFIED SERVICE PERSONNEL WITH EXPERTISE IN ELECTRONICS, MECHANICS, HYDRAULICS, CHEMISTRY, PNEUMATICS, AND OPTICS SHOULD USE THIS MANUAL TO PERFORM THE SERVICE SPECIFIED HEREIN. LACK OF SUCH EXPERTISE MIGHT RESULT IN PERSONAL INJURY AND/OR DAMAGE TO THE SYSTEM.

TABLE OF CONTENTS

Section	Title	Page
5A	MATERIALS REQUIRED	5-1
5B	SAMPLE & REAGENT PROBES	5-2
5B1	Summary of Preventive Maintenance	5-2
5B2	Cleaning New Sample & Reagent Probes	5-2
5B3	Cleaning Protein Buildup from Sample Probe	5-3
5B4	Alignment Check for Sample & Reagent Probes in Reaction Cuvettes	5-3
5B5	Alignment Check for Sample & Reagent Probes in Sample Cups & Reagent Boats	5-3
5B6	Reagent Probe Heater Check	5-3
5C	SAMPLE & REAGENT TURNTABLE	5-3
5C1	Summary of Preventive Maintenance	5-3
5C2	Check for Spillage	5-3
5C3	Operational Check	5-3
5D	SAMPLE & REAGENT PD PUMPS	5-3
5D1	Summary of Preventive Maintenance	5-3
5D2	Operational Check	5-4
5D3	Check for Syringe Leaks	5-4
5E	SAMPLE & REAGENT TRANSFER MECHANISMS	5-4
5E1	Summary of Preventive Maintenance	5-4
5E2	Operational Check	5-4
5F	REACTION MODULE	5-4
5F1	Summary of Preventive Maintenance	5-4
5F2	Drive Belt Check	5-4
5F3	Reaction Enclosure Air Seal Check	5-4
5F4	Alignment Check for Home & 90° Sensors	5-4
5F5	Operational Check	5-5
5G	COLORIMETER	5-5
5G1	Summary of Preventive Maintenance	5-5
5G2	Optics Lamp Voltage Check	5-5
5G3	Optics Lamp Replacement	5-5

5G4	Colorimeter Alignment	5-5
5G5	Colorimeter Filter Replacement	5-5
5H	AIR PUMP	5-6
5H1	Summary of Preventive Maintenance	5-6
5H2	Tubing Check	5-6
5H3	In-line Filter Replacement	5-6
5H4	Air Pressure Measurement	5-6
5H5	Air Pump Adjustment Procedure	5-6

TABLE OF CONTENTS (continued)

Section	Title	Page
5I	PERIPUMP	5-6
5I1	Summary of Preventive Maintenance	5-6
5I2	Platen Shaft Lubrication	5-6
5I3	Roller Alignment & Pump Operation Check	5-6
5J	PRINTER	5-7
5J1	Summary of Preventive Maintenance	5-7
5J2	Printer Tests	5-7
5K	TOUCH DISPLAY MODULE	5-7
5K1	Summary of Preventive Maintenance	5-7
5K2	Operational Check	5-7
5K3	Air Filter Cleaning	5-7
5K4	Touch Overlay Cleaning	5-8
5L	AIR INJECTORS	5-8
5L1	Summary of Preventive Maintenance	5-8
5L2	Air Injector Operational Check	5-8
5M	POWER SUPPLY & LINE VOLTAGES	5-8
5M1	Summary of Preventive Maintenance	5-8
5M2	Voltage Checks	5-8
5N	DISK DRIVE	5-8
5N1	Summary of Preventive Maintenance	5-8
5N2	Read/Write Head Cleaning Procedure	5-8
5O	TUBE REPLACEMENTS	5-9
5O1	Pump Tube Replacement	5-9
5O2	Air Tube Replacement	5-9
5P	RESERVOIR CUP REPLACEMENT	5-9
5Q	SYSTEM CLEANING PROCEDURE	5-9
5Q1	Internal System Cleaning	5-9
5Q2	Air Filter Cleaning	5-9
5R	SYSTEM PERFORMANCE CHECK	5-10
5R1	Materials Required	5-10
5R2	Abbreviated Auto Calibration Protocol	5-10
5R3	Glucose Calibration Protocol	5-10
5R4	Calculation	5-11
5R5	Procedure to Calculate Mean & SD	5-11
APPENDIX A	WORKSHEET FOR SYSTEM PERFORMANCE CHECK	5-12

LIST OF ILLUSTRATIONS

Figure	Title	Page
5B-1	Sample Probe Cleaning	5-2
5B-2	Reagent Probe Cleaning	5-2

5A MATERIALS REQUIRED

The following test equipment and consumables must be available before a preventive maintenance visit is made:

Test Equipment

- YSI 45 CU Thermometer
- YSI 4502 Probe
- Modified Reaction Tray Cover
- Marshall Town 83K (0-10 psi) Air Pressure Gauge
- DVM
- Oscilloscope
- Standard Electronics Tool Kit

Reagents and Consumables

- TESTpoint Assay Chemistry Control 1 (T03-1220) & TESTpoint Assay Chemistry Control 2 (T03-1221)
- Glucose Standard Solution T23-2803 from Calibration Kit T03-2802, or obtain equivalent from C.A.P., Publication Dept, 7400 N. Skokie Blvd., Skokie, IL 60077, Telephone 312-677-3500.
- In-line Air Filter P/N 518-3093-01
- Service Oil P/N 538-0015-01
- Standard Pump Tubes
- Colorimeter Lamp P/N 108-B310-01
- Colorimeter Filter Set P/N 192-R211-01
- Isopropyl Alcohol
- Syringe
- System Wash Solution T01-1287 (5% Sodium Hypochlorite - 40 g NaOH - Surfactant)

5B SAMPLE AND REAGENT PROBES

5B1 Summary of Preventive Maintenance

WARNING

To prevent eye damage, wear safety glasses.

	Maintenance	Material
1.	Clean sample and reagent probes.	10-mL syringe
2.	Check alignment of sample and reagent probes in reaction cuvettes.	0.030-inch gauge (P/N 192-R263-01)
3.	Check alignment of sample probe in sample cups, and reagent probe in reagent boats.	N/A
4.	Check reagent probe heater.	YSI 4502 Thermistor probe YSI 45 CU Thermometer Modified reaction tray cover

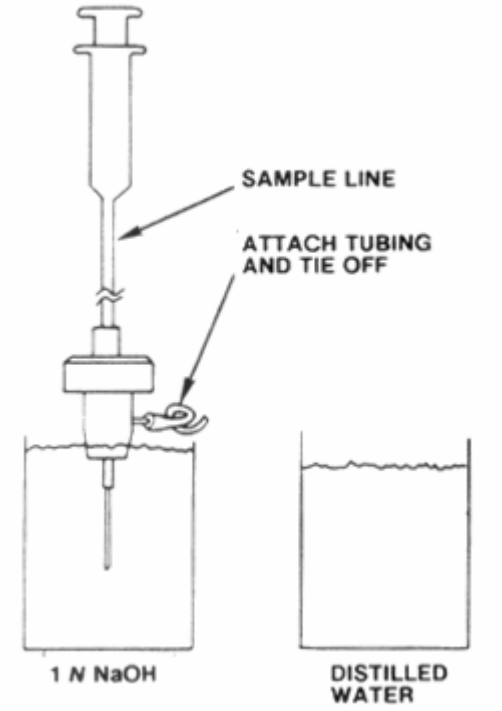


Figure 5B-1 SAMPLE PROBE CLEANING

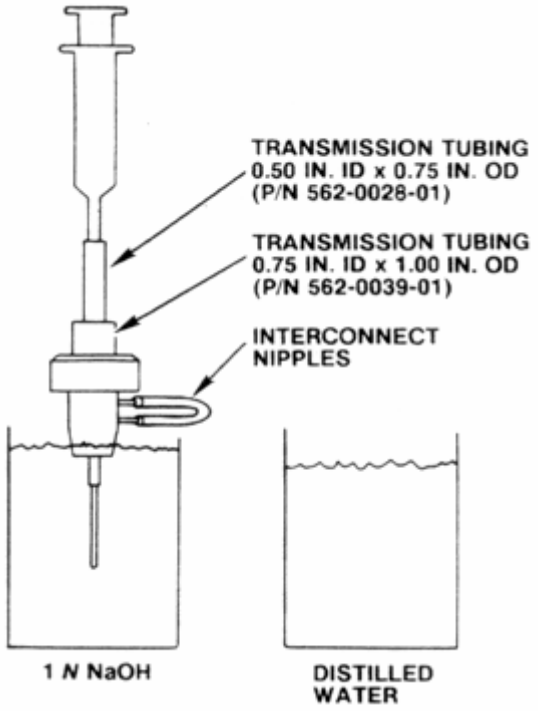

TRANSMISSION TUBING 0.50 IN. ID x 0.75 IN. OD (P/N 562-0028-01)
TRANSMISSION TUBING 0.75 IN. ID x 1.00 IN. OD (P/N 562-0039-01)
INTERCONNECT NIPPLES
1 N NaOH
DISTILLED WATER

Figure 5B-2 REAGENT PROBE CLEANING

5B2 Cleaning New Sample and Reagent Probes

1. Remove the sample probe assembly from the probe arm.
2. Connect a 10-mL syringe to the sample probe line as illustrated in Figure 5B-1. (Refer to Figure 5B-2 when cleaning reagent probes.)
3. Immerse the probe tip in a beaker filled with System Wash Solution (T01-1287).
4. Use the syringe to force wash solution back and forth through the probe for approximately five minutes. Occasionally remove the probe tip from the wash to aspirate air in 0.5-mL slugs (approx.). The air bubbles will help to scrub the inner walls.
5. Repeat Step 3 with distilled water. Rinse thoroughly.

6. Use a clean, filtered air source to dry the probe. When the probe is dry, it is ready for installation Do not touch probe tip with finger.
7. Before use, allow the probe to sit in the random access fluid reservoir for at least five minutes.

5B3 Cleaning Protein Buildup From Sample Probe

1. Wipe off residual random access fluid from the sample probe.
2. Rinse the probe thoroughly with distilled water.
3. Prime the probe with RA fluid. Before using, soak the probe in RA fluid reservoir for five minutes.

5B4 Alignment Check for Sample and Reagent Probes in Reaction Cuvettes

Verify that the sample and reagent probes do not make contact with the top or sides of the reaction cuvettes on entry. Make sure the probes are centered, and are at the proper height in the cuvette. If necessary, perform the alignment procedure contained in section 3B1 of this manual.

5B5 Alignment Check for Sample and Reagent Probes in Sample Cups and Reagent Boats

Verify that the sample and reagent probes are centered, and that they do not make contact with their respective receptacles. If necessary perform the alignment procedure contained in section 3B2 of this manual.

5B6 Reagent Probe Heater Check

Perform the temperature verification procedure contained in section 3F5 of this manual.

5C SAMPLE AND REAGENT TURNTABLES

5C1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Check for spillage	N/A
2.	Operational check	N/A

5C2 Check for Spillage

Clean the sample and reagent turntables with a damp cloth if there is any evidence of spillage.

5C3 Operational Check

Exercise the sample and reagent turntables. Verify that the turntables are not binding or operating erratically. Perform the sensor adjustments shown in section 3B2 of this manual.

5D SAMPLE AND REAGENT POSITIVE DISPLACEMENT PUMPS

5D1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Operational check	N/A
2.	Check for syringe leaks	N/A

5D2 Operational Check

Exercise the sample and reagent PD pumps. Verify that the pumps are not binding or operating erratically.

WARNING

Wear safety glasses to prevent eye injury.

5D3 Check for Syringe Leaks

Observe the syringe on each pump while it is operating, and check for leaks. If air leaks (producing microbubbles) are suspected in either syringe, the plunger, tip, and Tee fittings must be replaced, not the glass syringe body. The part number for the reagent plunger and tip assembly is P/N 510-4196-01. The part number for the sample plunger and tip assembly is P/N 510-4195-01. The part numbers for the sample and reagent pump Tee fittings are P/N 108-1272-01 and P/N 108-1272-02, respectively. Verify that the knurled screws at the bottom of the syringes are hand tightened.

5E SAMPLE AND REAGENT TRANSFER MECHANISMS

5E1 Summary of Preventive Maintenance

Maintenance	Material
Operational check	N/A

5E2 Operational Check

Exercise the sample and reagent probes. Verify that the transfer mechanisms are not binding or operating erratically.

5F REACTION MODULE

5F1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Check drive belt	N/A
2.	Check enclosure seal	N/A
3.	Check alignment of reaction	N/A
4.	Operational check	N/A

5F2 Drive Belt Check

Use the appropriate exerciser routine to step the reaction tray. Inspect the drive belt, and verify that it is not worn. Replace the belt if necessary.

5F3 Reaction Enclosure Air Seal Check

The reaction enclosure must be sealed properly to prevent warm air from escaping. Use a flashlight to locate leakage points between the upper and lower enclosure. Apply sealant where needed.

5F4 Alignment Check for the Home and 90?Sensors

WARNING

The following procedure will expose you to electrical shock hazard.

1. Use an oscilloscope to monitor the home and 90?sensors (see Figure 3C-2).
2. Using the exerciser, home the reaction tray. At the HOME position, both oscilloscope traces should shift upward simultaneously. "HOME" should be displayed on the Touch Display Module.
3. To determine the center of the sensor disk cutout, step the reaction tray three half-steps in one direction. The oscilloscope traces should drop to zero volts. Step the reaction tray back three steps until "HOME" is again displayed on the Touch Display Module. Step the reaction tray four steps in the other direction. The oscilloscope traces should drop to zero volts on the fourth step. If necessary realign the reaction tray sensors as described in section 3C of this manual.

5F5 Operational Check

Using the exerciser, select the following reaction tray tests: home, slew, mix, and index. Check that the reaction tray is not binding or operating erratically.

5G COLORIMETER

5G1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Lamp voltage measurements	DVM
2.	Optics lamp replacement	Colorimeter lamp (P N 108-B310-01)
3.	Colorimeter alignment	DVM & Alignment pin

5G2 Optics Lamp Voltage Check

With the system in STANDBY, verify that the voltage at TB1 on the colorimeter assembly is 7.2 V dc ?0.05 V dc. Adjust the 7.2-V d-c power supply if necessary.

NOTE

The lamp voltage should remain at 7.2 V dc when the system is placed in the READY and OPERATE modes.

5G3 Optics Lamp Replacement

1. Shut OFF system power. Unplug the power cord.
2. Disconnect the two colorimeter lamp wires from terminal block A8TB1.
3. Loosen the captive screws that secure the lamp holder to the lamp housing assembly.
4. Install the replacement colorimeter lamp. Be sure that the lamp alignment studs are properly set in the slots in the lamp housing before tightening the captive screws.

CAUTION

To prevent damage to the lamp, avoid placing fingers the glass portion of the lamp.

5. Apply power.

5G4 Colorimeter Alignment

Perform the alignment procedures contained in sections 3D1 and 3D2.

5G5 Colorimeter Filter Replacement

Perform the procedure contained in section 3D5.

5H AIR PUMP

5H1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Check tubing	N/A
2.	Replace in-line filter	Filter P/N 518-3093-01
3.	Check air pressure	Air pressure gauge (83K) 0-10 Ib, Marshall Town pressure gauge recommended.

WARNING

Servicing the air pump will expose you to electrical shock hazard.

5H2 Tubing Check

Check that the tubing from the air pump to the reagent probe is unobstructed and in good condition.

5H3 In-line Filter Replacement

Replace the in-line air filter (P/N 518-3093-01).

5H4 Air Pressure Measurement

With the air pump operating, connect the gauge to the output of the pump assembly and measure the air pressure. It should be 5 PSI ?10%. If the air pressure is too low, check for air leaks. If the air pressure is too high, the pump stroke must be adjusted.

5H5 Air Pump Adjustment Procedure

1. Loosen the pump motor hold down screws.
2. With the pump operating, slide the motor up to increase (or down to decrease) the air pressure. Tighten the hold down screws when the proper air pressure is attained.

5I PERIPUMP

5I1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Lubricate platen shaft	Service Oil P/N 538-0015-01
2.	Check pump operation and alignment of rollers.	N/A

5I2 Platen Shaft Lubrication

1. Set pump platen lever to the released (up) position.
2. Apply two drops of Prolonged Service Oil (P/N 538-0015-01) along the platen shaft.
3. Raise and lower the platen several times to uniformly oil the shaft.

5I3 Roller Alignment and Pump Operation Check

1. Exercise the peripump motor. When the pump stops, one of the four rollers should be at the center of the platen.

2. If the roller is off center, adjust the sensor until the proper position is attained.
3. Check that the pump is not binding or operating erratically.

5J PRINTER

5J1 Summary of Preventive Maintenance

Maintenance	Material
Check print quality	N/A

5J2 Printer Tests

Perform the printer tests described in section 3E. Replace the printer controller board or printer if necessary.

5K TOUCH DISPLAY MODULE

5K1 Summary of Preventive Maintenance

	Maintenance	Material
1.	Check operation	N/A
2.	Clean air filter	N/A
3.	Clean Touch Overlay	Lightly moistened nonabrasive cloth

5K2 Operational Check

Complete steps 1 through 4 of the Performance Test contained in Section 6 of the *Fluke 1780A Info Touch Display Instruction Manual.* If necessary, perform the calibration procedures contained in Section 6 of the Fluke manual.

The Performance Test requires manipulation of the switches at the rear of the module. The normal settings of the switches for use with the RA-XT system are:

Switch Sl:

POSITION	SETTING	FUNCTION
1	Down	No Parity
2	Down	Odd/Even
3	Down	1 Stop Bit
4	Up	8 Data Bits
5	Down	Test Mode OFF
6	Down	Auto LF OFF
7	Down	Auto Wrap-Around OFF

Switch S2:

Position 7 (9600 Baud Rate)

5K3 Air Filter Cleaning

1. With the Touch Display Module power off, remove the air filter from the rear panel.
2. Wash the filter in warm soapy water; rinse it with clean water.
3. Blot the filter dry.

5K4 Touch Overlay Cleaning

Use a soft, lightly moistened cloth and a mild soap solution to clean the overlay. Do not allow the soap solution to drip down into the CRT enclosure.

5L AIR INJECTORS

5L1 Summary of Preventive Maintenance

Maintenance	Material
Check operation	N/A

5L2 Air Injector Operational Check

Exercise the pinch valves, and verify that they are operating properly.

5M POWER SUPPLY AND LINE VOLTAGES

5M1 Summary of Preventive Maintenance

Maintenance	Material
Check voltages	DVM

5M2 Voltage Checks

WARNING

Checking voltages will expose you to electrical shock hazard.

Refer to Power Distribution Drawing 108-C807, and check the line voltages. Check the PS1 and PS2 outputs.

5N DISK DRIVE

5N1 Summary of Preventive Maintenance

Maintenance	Material
Clean read/write head	Isopropyl alcohol

5N2 Read/Write Head Cleaning Procedure

CAUTION

The head should be cleaned only if it has an oxide buildup that is visible to the naked eye. Cleaning methods and materials other than those specified can permanently damage the head, and should be avoided.

1. Lightly dampen a piece of clean, lint-free tissue paper with isopropyl alcohol (use sparingly).
2. Lift the upper arm assembly.
3. Lightly wipe the head with the moistened portion of tissue.
4. After alcohol has evaporated, lightly polish head with a clean, dry piece of lint-free tissue. Clean off all residue.

5O TUBE REPLACEMENTS

5O1 Pump Tube Replacement

To replace peripump tubes:

1. Raise the pump platen.
2. Replace pump tubes P/N 178-3748-04 (3 each) and P/N 178-3748-09 (1 each). Refer to Figure 5O-1.
3. Set pump platen down.

5O2 Air Tube Replacement

With the system power off, install a new air tube on the air injection pinch valves. Refer to the TECHNICON RA-XT System *Illustrated Parts Manual,* Figures 3 and 21 for part numbers and installation notes.

5P RESERVOIR CUP REPLACEMENT

1. Use the exerciser to raise the sample and reagent probes.
2. Replace both reservoir cups (P/N 108-1348-01).
3. Fill each cup with Random Access Fluid.

5Q SYSTEM CLEANING PROCEDURE

5Q1 Internal System Cleaning

Vacuum or clean with a towel all internal areas of the system.

5Q2 Air Filter Cleaning

1. Shut OFF system power.
2. Remove blower filters for fan assemblies B1, B2, B3, and B6.
3. Use a vacuum or mild soap solution to clean blower filters. Dry the filters if necessary.
4. Reinstall blower filters.

5R SYSTEM PERFORMANCE CHECK

5R1 Materials Required

- TESTpoint Assay Chemistry Control 1 (T0S-1220) & TESTpoint Assay Chemistry Control 2 (T03-1221)
- Glucose Standard Solution T23-2803 or equivalent

5R2 Abbreviated Auto Calibration Protocol

1. Perform the glucose calibration procedure outlined in section 5R3 below.
2. Run TESTpoint controls on the following chemistries:
   a. LDH
   b. GGT
   c. Alk Phos
   d. BUN
   e. Glucose

CAUTION

TESTpoint controls must be fresh (made within one half hour of use).

3. Record in Tables I and II in Appendix A the retrieved values from steps 1 and 2. Attach the insert to the Protocol. Compare the measured mean value with the accuracy range specified. Troubleshoot any chemistry that does not meet the insert value and repeat the protocol (include both sets of data).
4. Refer to section 5R5 for procedures to calculate means and standard deviations.

5R3 Glucose Calibration Protocol

1. Create a user-defined end point chemistry with the following parameters:

TYPE	ENDPOINT
% SAMPLE VOLUME	7
WAVELENGTH	340
DELAY TIME	5:00
% REAGENT VOLUME	70
UNITS	MG/DL
UNIT FACTOR	1
DECIMAL POINT	4
RBL LOW	0
RBL HIGH	1
RANGE LOW	0
RANGE HIGH	1
CALIBRATION FACTOR	1
STANDARD VALUE	0
NORMAL LOW	0
NORMAL HIGH	1
SLOPE	1
INTERCEPT	0
ENDPOINT LIMIT	1

NOTE

After the last entry, the above parameters will be printed out automatically.

2. Fill eleven (11) 0.5-mL sample cups with the Glucose Standard Solution.

3. Perform one assay on each cup of Glucose Standard Solution, using RA Systems Glucose Reagent T01-1825-56 (20 mL/vial).

5R4 Calculation

1. Discard the first value obtained (from cup 1).
2. Calculate the mean and standard deviation of the last ten (10) absorbances (see next section).
3. If the standard deviation is less than 0.025 absorbance unit (*A*), continue; otherwise, repeat the 11 assays.
4. Multiply the average absorbance by 12,520 to obtain the extinction coefficient (E).
5. If the extinction coefficient (E) is less than 6,000 or greater than 6600, contact your local Technicon Technicenter office.
6. Attach a copy of the results to the System Maintenance Log. Return a copy to your Technicenter.

5R5 Procedure to Calculate Mean and Standard Deviation

Mean:

Add up the assay values produced by cups 2-11 (10 numbers total) then divide by 10.

Standard Deviation:

1. For each assay value produced by cups 2-11, calculate the difference from the mean value.

   Example: Mean Value = 214
   Cup #2 Assay Value = 200
   Difference = 14

2. Square the difference.

   Example: 14 x 14 = 196

3. Add all squared numbers together, and divide the total by 10.
4. Take the square root of the number obtained in step 3. This is the standard deviation.

APPENDIX A
WORKSHEET FOR SYSTEM PERFORMANCE CHECK

TESTpoint 1 LOT # _____

TESTpoint 2 LOT # _____

TABLE I RETRIEVED GLUCOSE VALUES

CUP*	MEAN DIFFERENCE	SQUARED DIFFERENCE
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
Mean		
SD		

* Do not use cup # in calculations

TABLE II TESTpoint CONTROL VALUES

CHEMISTRY	CONTROL	LABELED VALUE	RETRIEVED VALUE
LD	TESTpoint 1		
	TESTpoint 2		
GGT	TESTpoint 1		
	TESTpoint 2		
ALK	TESTpoint 1		
	TESTpoint 2		
BUN	TESTpoint 1		
	TESTpoint 2		
GLUCOSE	TESTpoint 1		
	TESTpoint 2		

CHAPTER SIX

SCHEMATICS

WARNING

ONLY QUALIFIED SERVICE PERSONNEL WITH EXPERTISE IN ELECTRONICS, MECHANICS, HYDRAULICS, CHEMISTRY, PNEUMATICS, AND OPTICS SHOULD USE THIS MANUAL TO PERFORM THE SERVICE SPECIFIED HEREIN. LACK OF SUCH EXPERTISE MIGHT RESULT IN PERSONAL INJURY AND/OR DAMAGE TO THE SYSTEM.

TABLE OF CONTENTS

Drawing Number	Title	Page
108-C037	Reagent & Sample Dispensing A1	6-1
108-C050	Hydraulic-Pneumatic Interconnect Diagram	6-2
108-C063	Alarm Control Board	6-3
108-C075	Detector Amplifier	6-4
108-C083	7.2 V dc Supply Board	6-5
108-C097	Stepper Motor Sensor Board	6-6
108-C104	Air Injection Control Board	6-7
108-C108	AC Motor & Sensor Control Board	6-8
108-C126	7.2 V dc Power Supply	6-9
108-C146	Analog/Digital Converter	6-10
108-C148	CPU/Memory/Disk Controller Board	6-11
108-C152	Colorimeter	6-16
108-C153	Reaction Tray Module	6-17
108-C157	Sample Turntable	6-18
108-C158	Reagent Turntable	6-19
108-C162	Resistor Heat Sink Assembly	6-20
108-C186	Data Acquisition Board	6-21
108-C189	Stepper Motor Controller Board	6-23
108-C197	Stepper Motor Sensor Board	6-26
108-C198	Serial I/O Board	6-27
108-C199	AC Motor Control Board	6-29
108-C229	DC Motor & Sensor Control Board	6-32
108-C273	IDee Module Voltage Regulator Assembly	6-33
108-C278	Transfer Mechanism	6-34
108-C407	ISE Heat Sink Component Board	6-35
108-C408	ISE Interconnect Diagram	6-36
108-C410	ISE CPU Control Board	6-37
108-C413	ISE Power Distribution	6-40
108-C432	Hydraulic-Pneumatic Interconnect Diagram (ISE)	6-42
108-C433	ISE Data Acquisition Board	6-43
108-C452	ISE Display Board	6-44
108-C458	Sample & Reagent Transfer Mechanism	6-45
108-C463	ISE Amplifier	6-46

108-C800	Reagent Encoder (24 Pos.) - Lower	6-48
108-C801	Reagent Encoder (24 Pos.) - Upper	6-49
108-C803	Scrambler Board	6-50
108-C804	RAM Disk Board	6-51
108-C806	Interconnect Cable Diagram	6-53
108-C807	Power Distribution	6-56
108-C809	Indicator Panel	6-59
108-C810	Scrambler Board	6-60
108-C822	Temperature Controller	6-61

SCHEMATIC - REAGENT & SAMPLE DISPENSING A1
DWG. NO. 108-C037 (REV. F)

HYDRAULIC - PNEUMATIC INTERCONNECT SCHEMATIC
DWG. NO. 108-C050

SCHEMATIC ALARM CONTROL BOARD
DWG. NO. 108-C063 (REV. F)

SCHEMATIC - DETECTOR AMPLIFIER
DWG. NO. 108-C075 (REV. F)

SCHEMATIC, P.C. BOARD 7.2 VDC PWR. SUPPLY, WEDNESDAY
DWG. NO. 108-C083 (REV. B)

SCHEMATIC - STEPPER MOTOR / SENSOR P.C. BOARD
DWG. NO. 108-C097 (REV. G)

SCHEMATIC - AIR INJECTION CONTROL P.C. BOARD
DWG. NO. 108-C104 (REV. K)

SCHEMATIC - A.C. MOTOR & SENSOR CONTROL BOARD
DWG. NO. 108-C108 (REV. G)

+ 7.2 VDC POWER SUPPLY SCHEMATIC
DWG. NO. 108-C126

SCHEMATIC ANALOG/DIGITAL CONVERTER
DWG. NO. 108-C146 (REV. E)

SCHEMATIC - CPU/MEMORY/DISK CONTROLLER BOARD
DWG. NO. 108-C148 (REV. H)
SHEET 1 OF 5

SCHEMATIC - CPU/MEMORY/DISK CONTROLLER BOARD
DWG. NO. 108-C148 (REV. H)
SHEET 2 OF 5

SCHEMATIC - CPU/MEMORY/DISK CONTROLLER BOARD
DWG. NO. 108-C148 (REV. H)
SHEET 3 OF 5

SCHEMATIC - CPU/MEMORY/DISK CONTROLLER BOARD
DWG. NO. 108-C148 (REV. H)
SHEET 4 OF 5

SCHEMATIC - CPU/MEMORY/DISK CONTROLLER BOARD
DWG. NO. 108-C148 (REV. H)
SHEET 5 OF 5

SCHEMATIC - COLORIMETER
DWG. NO. 108-C152 (REV. C)

SCHEMATIC - REACTION TRAY MODULE
DWG. NO. 108-C153

SCHEMATIC - A7 SAMPLE TURNTABLE
DWG. NO. 108-C157 (REV. D)

SCHEMATIC - A6 REAGENT TURNTABLE
DWG. NO. 108-C158 (REV. C)

SCHEMATIC - RESISTOR HEAT SINK ASSEMBLY
DWG. NO. 108-C162 (REV. K)

SCHEMATIC - DATA ACQUISITION BOARD
DWG. NO. 108-C186 (REV. D)
SHEET 1 OF 2

SCHEMATIC - DATA ACQUISITION BOARD
DWG. NO. 108-C186 (REV. D)
SHEET 2 OF 2

SCHEMATIC - STEPPER MOTOR CONTROLLER & FRONT PANEL
DWG. NO. 108-C189 (REV. J)
SHEET 1 OF 3

SCHEMATIC - STEPPER MOTOR CONTROLLER & FRONT PANEL
DWG. NO. 108-C189 (REV. J)
SHEET 2 OF 3

SCHEMATIC - STEPPER MOTOR CONTROLLER & FRONT PANEL
DWG. NO. 108-C189 (REV. J)
SHEET 3 OF 3

SCHEMATIC - STEPPER MOTOR/SENSOR P.C. BOARD
DWG. NO. 108-C197 (REV. C)

SCHEMATIC - SERIAL I/O BOARD
DWG. NO. 108-C198 (REV. L)
SHEET 1 OF 2

SCHEMATIC - SERIAL I/O BOARD
DWG. NO. 108-C198 (REV. L)
SHEET 2 OF 2

SCHEMATIC - A.C. MOTOR CONTROL BOARD
DWG. NO. 108-C199 (REV. G)
SHEET 1 OF 3

SCHEMATIC - AC MOTOR CONTROL BOARD
DWG. NO. 108-C199 (REV. G)
SHEET 2 OF 3

SCHEMATIC - AC MOTOR CONTROL BOARD
DWG. NO. 108-C199 (REV. G)
SHEET 3 OF 3

SCHEMATIC - D.C. MOTOR & SENSOR CONTROL BOARD
DWG. NO. 108-C229 (REV. G)

SCHEMATIC - IDEE MODULE VOLTAGE REGULATOR ASSEMBLY
DWG. NO. 108-C273 (REV. C)

SCHEMATIC - TRANSFER MECHANISM
DWG. NO. 108-C278 (REV. F)

SCHEMATIC - I.S.E HEAT SINK COMPONENT BOARD. ASSY.
DWG. NO. 108-C407 (REV. B)

RA-100 ISE INTERCONNECT CABLE DIAGRAM
DWG. NO. 108-C408 (REV. K)

SCHEMATIC - ISE CPU CONTROL BOARD
DWG. NO. 108-C410 (REV. J)
SHEET 1 OF 3

SCHEMATIC - ISE CPU CONTROL BOARD
DWG. NO. 108-C410 (REV. J)
SHEET 2 OF 3

SCHEMATIC - ISE CPU CONTROL BOARD
DWG. NO. 108-C410 (REV. J)
SHEET 3 OF 3

SCHEMATIC - RA 1000 ISE POWER DISTRIBUTION
DWG. NO. 108-C413 (REV. H)
SHEET 1 OF 2

SCHEMATIC - RA 1000 ISE POWER DISTRIBUTION
DWG. NO. 108-C413 (REV. H)
SHEET 2 OF 2

HYDRAULIC - PNEUMATIC INTERCONNECT SCHEMATIC
DWG. NO. 108-C432

SCHEMATIC - ISE DATA ACQUISITION BOARD
DWG. NO. 108-C433 (REV. F)

SCHEMATIC - ISE DISPLAY BOARD
DWG. NO. 108-C452 (REV. B)

SCHEMATIC - SAMPLE & REAGENT TRANSFER MECHANISM
DWG. NO. 108-C458 (REV. F)

SCHEMATIC - ISE AMPLIFIER
DWG. NO. 108-C463 (REV. F)
SHEET 1 OF 2

SCHEMATIC - ISE AMPLIFIER
DWG. NO. 108-C463 (REV. F)
SHEET 2 OF 2

SCHEMATIC - REAGENT ENCODER (24 POS.) - LOWER
DWG. NO. 108-C800 (REV. C)

SCHEMATIC - REAGENT ENCODER (24 POS.) - UPPER
DWG. NO. 108-C801 (REV. B)

SCHEMATIC - SCRAMBLER BOARD
DWG. NO. 108-C803 (REV. B)

SCHEMATIC - RAM DISK BOARD
DWG. NO. 108-C804 (REV. F)
SHEET 1 OF 2

SCHEMATIC - RAM DISK BOARD
DWG. NO. 108-C804 (REV. F)
SHEET 2 OF 2

RA-XT INTERCONNECT CABLE DIAGRAM
DWG. NO. 108-C806 (REV. J)
SHEET 1 OF 3

RA-XT INTERCONNECT CABLE DIAGRAM
DWG. NO. 108-C806 (REV. J)
SHEET 2 OF 3

RA-XT INTERCONNECT CABLE DIAGRAM
DWG. NO. 108-C806 (REV. J)
SHEET 3 OF 3

SCHEMATIC - RA-XT POWER DISTRIBUTION
DWG. NO. 108-C807 (REV. H)
SHEET 1 OF 3

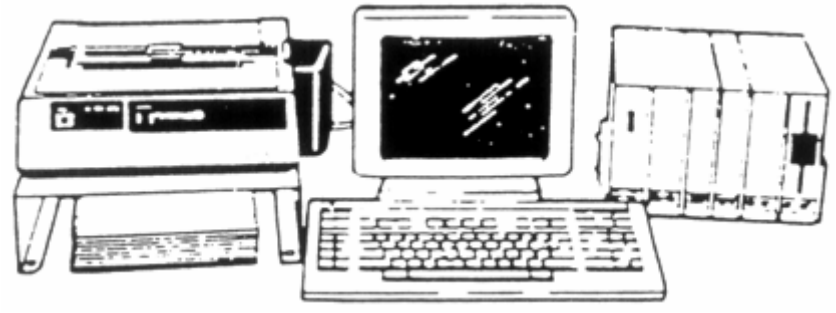
SCHEMATIC - RA-XT POWER DISTRIBUTION
DWG. NO. 108-C807 (REV. H)
SHEET 2 OF 3

SCHEMATIC - RA-XT POWER DISTRIBUTION
DWG. NO. 108-C807 (REV. H)
SHEET 3 OF 3

SCHEMATIC - INDICATOR PANEL
DWG. NO. 108-C809 (REV. B)

SCHEMATIC - SCRAMBLER BOARD
DWG. NO. 108-C810 (REV. B)

SCHEMATIC - TEMPERATURE CONTROLLER
DWG. NO. 108-C822 (REV. D)



Service Manual NGEN Workstation

TECHNICON®

Specifications Subject to Change.

Convergent Technologies, Convergent, CTOS, CT-BUS, CT-DBMS, CT-MAIL, CT-Net, DISTRIX, AWS, IWS, and NGEN are trademarks of Convergent Technologies, Inc.

CP / M-86 is a trademark of Digital Research.
MS, GW and XENIX are trademarks of Microsoft Corp.
UNIX is a trademark of Bell Laboratories.

Second Edition (November 1984) A-09-00908-01-A

Copyright ?1983, 1984
by Convergent Technologies, Inc.

All rights reserved. Title to and ownership of the documentation contained herein shall at all times remain in Convergent Technologies, Inc., and / or its suppliers. The full copyright notice may not be modified except with the express written consent of Convergent Technologies, Inc.

CONTENTS

SUMMARY OF CHANGES vii

RELATED DOCUMENTATION viii

1 OVERVIEW 1-1
INTRODUCTION TO DIAGNOSTICS 1-1
MANUAL ORGANIZATION 1-1

2 USING THE DIAGNOSTICS 2-1
INTRODUCTION 2-1
BOOTSTRAPPING THE DIAGNOSTICS 2-2
Vendor Code and Bad Spot Data 2-2
Bootstrapping the Diagnostics from a Floppy Disk 2-3
SCREEN FORMAT 2-4
CONFIGURATION DISPLAY 2-4
Power Check 2-5
Configuration Rules Check 2-5
SELECTING HARDWARE MODULES FOR TEST 2-6
Selecting Submodules Within a Module for Test 2-7
Initial Dialogue 2-8
STARTING THE TESTS 2-9
Video Displays During and After the Tests 2-9
Keyboard Interaction During the Tests 2-10

3 PROCESSOR MODULES 3-1
MEMORY EXPANSION CARTRIDGE TESTS 3-1
RS-232-C TESTS 3-3
Error Information Screen 3-6
Error Information 3-6
Probable Causes of the Error 3-7
RS-232-C Interface Chip (8274) Status Information 3-7
Extended Status Register Information 3-7
Dialogue 3-7
RS-422 (CLUSTER COMMUNICATIONS) TESTS 3-7
PARALLEL I/O (PRINTER) TESTS 3-9
Printer Error Messages 3-10
BASE MEMORY TEST 3-11
CPU TIMER TEST 3-11

VIDEO CONTROLLER TEST 3-11
Video Memory Test 3-12
Video Attribute Test 3-12
Font Display Test 3-12
Mosquito Net Test 3-12
Cursored String Test 3-13

4 MULTILINE PORT EXPANDER MODULE TESTS 4-1

5 DISK MODULES 5-1
DUAL FLOPPY DISK MODULE 5-1
Introduction 5-1
Floppy Disk Tests 5-1
Selecting Individual Tests 5-4
Error Message Format 5-9
FLOPPY/HARD DISK MODULE 5-10
Introduction 5-10
Floppy Disk Tests 5-10
Hard Disk Tests 5-11
Selecting Individual Tests 5-15
Error Message Format 5-20
DISK UPGRADE AND DISK EXPANSION MODULES TESTS 5-21

6 MONITORS 6-1
MONOCHROME MONITOR TESTS 6-1
COLOR MONITOR TESTS 6-2
Color Bar Test 1 6-3
Color Bar Test 2 6-3
Speaker Test 6-4

7 GRAPHICS CONTROLLER MODULE 7-1
INTRODUCTION 7-1

8 TELEPHONE MANAGER MODULE 8-1
INTRODUCTION 8-1

9 KEYBOARD 9-1
INTRODUCTION 9-1
KEYBOARD TESTS 9-1
I-Bus Hardware Reset 9-2
ID Sequence 9-2
KBD Software Reset 9-3
ROM Checksum 9-3
Loopback Test 9-3

APPENDIX A: DIAGNOSTICS SELECTION PROGRAM (SP) A-1

GLOSSARY Glossary-1

INDEX Index-1

SUMMARY OF CHANGES

The 2.0 Release of Visinostics is described in this second edition of the Diagnostics Manual (A-09-00908-01-A). This edition differs from the first edition in two main ways.

- New material has been added to document changes to individual diagnostic tests and to expand the diagnostics descriptions to cover modules not included in the first edition.
- The manual has been reorganized to make it easier to use.

NEW MATERIAL

The new modules covered in this edition are

- Multiline Port Expander Module
- Monitors
- Graphics Controller Module
- Telephone Manager Module

The new information for these modules is described in the "Reorganization" subsection. In addition to documentation for new modules, this edition also contains updated descriptions of the diagnostic tests for Processor Modules, disk modules, and the keyboard.

REORGANIZATION

The manual has been reorganized to make the diagnostics descriptions for each type of module easier to access. The diagnostics descriptions are now covered in new sections organized by module type. For ease of reference, each type of module has its own section. Each section is briefly described below.

Note that the bootstrap ROM firmware documentation contained in the first edition has been removed. For general information on the bootstrap ROM firmware and descriptions of bootstrap ROM errors, see the Status Codes Manual. For information on the panel Debugger routine, see the Processor manual for your system.

RELATED DOCUMENTATION

SECTION 2, "USING THE DIAGNOSTICS"

This section is now devoted to general topics such as bootstrapping the diagnostics, selecting hardware modules for test, and starting the tests. Documentation for individual tests and the diagnostics Selection Program (SP) have been removed to form new sections as described below.

SECTION 3, "PROCESSOR MODULES"

This section describes the Processor Module tests. The video tests have been added to this section in the "Video Controller Test" subsection.

SECTION 4, "MULTILINE PORT EXPANDER MODULE TESTS"

This section is new material. It describes the tests for this module and refers you to the "RS-232-C Tests" subsection of Section 3, "Processor Modules" for more details.

SECTION 5, "DISK MODULES"

This section describes the diagnostic tests for Dual Floppy Disk Modules, Floppy/Hard Disk Modules, Disk Upgrade Modules, and Disk Expansion Modules.

SECTION 6, "MONITORS"

The material in this section is all new. The "Monochrome Monitors" subsection refers you to the "Video Controller Test" subsection of Section 3, "Processor Modules," and the "Color Monitor" subsection describes new tests.

SECTION 7, "GRAPHICS CONTROLLER MODULE"

The material in this section is all new. The introduction explains the differences between tests run on a Monochrome Monitor and tests run on a Color Monitor. All the new Graphics Controller Module tests are included.

SECTION 8, "TELEPHONE MANAGER MODULE"

The material in this section is all new. The tests for the Telephone Manager Module are described.

SECTION 9, "KEYBOARD"

The material in this section updates the test description in the previous edition to reflect changes in the screen prompts.

APPENDIX A: DIAGNOSTICS SELECTION PROGRAM (SP)

This material has not changed, but has been placed in its own section as an appendix for ease of reference.

1 OVERVIEW

INTRODUCTION TO DIAGNOSTICS

The diagnostics is a self-contained package of tests used to check the modular components of your workstation. Most of the tests are self-checking, and once started, run without the need for user intervention. Little more is required than to start up the system, load the diagnostics, and answer the preliminary questions. The diagnostics automatically tell you, by means of a message on the screen, which of your components have passed and which have failed.

Those module tests that are not self-checking are clearly pointed out in the documentation. These tests require visual verification while they are being run.

The diagnostics is designed to be used by systems administrators. It provides complete tests for every module in your system and should be the first piece of software run when the workstation is assembled.

However, it is not meant to be a troubleshooting package, and should be used with this in mind. If a problem is found, consult a field service technician familiar with your system.

MANUAL ORGANIZATION

Section 1 is a brief introduction to this manual.

Sections 2 through 9 describe in detail how the tests are used.

Appendix A describes the Selection Program (SP), an application program that allows you to preconfigure the diagnostics for a particular purpose.

2 USING THE DIAGNOSTICS

INTRODUCTION

The diagnostic tests are chosen and executed by means of a single pictorial menu. This icon menu displays pictures (icons) of the modules connected to your workstation system. You mark the appropriate modules and submodules, then run the tests by pressing GO. The diagnostics can be chosen in any combination and runs only those tests that are marked.

Once the icon menu appears on the screen, you must verify that it has recognized all the modules present in your system. Each icon looks similar to the actual module, and each has a name displayed above it. Thus it is an easy matter to count the icons and match them to the modules present. If the icons do not match your system, see the subsections "Configuration Display" and "Power Check" below.

Some Processor Modules do not require power or configuration checks. In these cases, there can be no violation of the configuration rules.

If a configuration rule has been violated, such as having Memory Expansion Cartridges installed nonsequentially in a Processor Module, the diagnostics displays the error as a written message before the tests take place. We recommend that configuration violations be remedied before continuing with the diagnostics.

> CAUTION
>
> The floppy disk and hard disk tests destroy the data in both drives. Hard disks should be backed up before running the diagnostics. After bootstrapping, scratch disks should be inserted in the floppy disk drives.

BOOTSTRAPPING THE DIAGNOSTICS

Before bootstrapping the diagnostics, verify that all modules and components are properly connected.

The diagnostics can be loaded into your system in one of two ways:

- If your system is part of a cluster, the diagnostics can be bootstrapped from a master workstation. It can also be bootstrapped from your workstation's floppy disk drive. To install the diagnostics on a master and bootstrap over the cluster line, see the current "Release Notice for Standard Software" for your system.

- If your system is a standalone workstation, the diagnostics must be bootstrapped from a floppy disk via your workstation's floppy disk drive. (See the subsection "Bootstrapping the Diagnostics from a Floppy Disk.")

VENDOR CODE AND BAD SPOT DATA

The bottom of every disk drive chassis has a label with important information needed to run the diagnostics. This label holds the vendor code letter and the bad spot data for the disk. This information should be written down in its entirety before bootstrapping and saved until the disk drive portion of the tests is performed.

The following information should be noted:

- the number of cylinders
- the number of write/read heads
- the number of sectors per track

Noting this information now saves you from having to turn over the disk modules when the disk drive tests are run.

If there are no bad spots on the disk, the label says "No media defects."

For further information about vendor codes and bad spot data, see the subsection "Floppy/Hard Disk Module Tests," in Section 5, "Disk Modules."

NOTE

An error code 20h (E:20) when bootstrapping the diagnostics indicates an incompatibility between your Processor Module and the disk drives used in your system. If you receive an error code 20h, see the Status Codes Manual, or contact a field service technician for further information about the problem.

BOOTSTRAPPING THE DIAGNOSTICS FROM A FLOPPY DISK

To bootstrap the diagnostics from a floppy disk,

1. Turn on the power switch on the front of the Processor Module.
2. Hold down the spacebar.
3. Press the reset button on the back of the Processor Module. It is on the top left side.
4. Release the reset button and wait until the bootstrap menu appears (B,D,L,M,P,T:).
5. Let go of the spacebar.
6. Insert the diagnostics disk in the leftmost floppy disk drive, with the write-protect notch facing up.
7. Close the floppy disk drive door.
8. Press B on the keyboard to select bootstrap from the bootstrap menu.
9. The diagnostics automatically bootstraps from the floppy disk, and the icon menu appears.

If the floppy disk does not bootstrap, check the power and X-Bus connections to your modules or call a field service technician familiar with your workstation.

SCREEN FORMAT

The diagnostics divides the screen into three horizontally separated windows as follows:

O The top window

- contains a legend that indicates the attribute state of the diagnostics (for example, testing, successful, failed)
- spells out the type of processor being used by your workstation
- shows the keystrokes used to move around inside the program

O The middle window is where the diagnostic queries appear and the tests are run. It scrolls upward as the diagnostics proceeds. In the monitors and graphics controller portions of the tests this scrolling can be stopped or started by pressing PREV PAGE and NEXT PAGE, respectively.

O The bottom window displays the hardware configuration (the icon menu) and the status of the currently selected tests. Soft and hard (intermittent and definite) errors are shown under each icon as they occur during the testing cycle.

Certain tests change the screen while they are being run. The screen returns to normal when the tests are complete.

CONFIGURATION DISPLAY

After the diagnostics has been bootstrapped, and the screen format appears, the first thing you see is the icon menu and a request to verify the power provided to your modules. These are seen in the bottom window.

The icon menu shows, from left to right, the modules that are present on the X-Bus, the monitor, and the keyboard. The display details the memory configuration of the Processor Module and distinguishes between different types of monitors.

In all but very large configurations, the entire arrangement fits into the bottom window of the screen. However, if three dots (...) appear at the right or left edge of the display, there are additional modules that could not be shown. In this case, the entire display can be shifted by moving the cursor to the extreme right or left side using the right or left arrow keys.

POWER CHECK

If the display does not correspond to the actual arrangement of your modules, check the power configuration. In most cases, failure to properly supply power to a module or group of modules can cause the modules to go unnoticed by the system.

The required location of the 36-Volt Power Supply bricks are shown by flashing plug symbols beneath the appropriate modules. Make sure the indicated modules are each connected to a 36-Volt Power Supply brick, and that the bricks are plugged into each other or into a wall outlet. If no plug symbol is seen beneath a module, no 36-Volt Power Supply brick is required.

You are responsible for verifying that adequate power is supplied to your modules. This ensures the proper operation of the diagnostics. If the required power is not supplied, the system still operates but may malfunction.

After making sure the power configuration is correct, press any key to continue. The power plug symbols will stop flashing.

For further information about power requirements for the workstation, see the Power System Manual.

CONFIGURATION RULES CHECK

If a configuration rule is violated, a message describing the violation appears on the screen. If no message appears, there is no violation. An example of a configuration rule that may be violated is the overall length of the X-Bus. From the right side of the Processor Module to the left side of the last module, the length of the X-Bus should not exceed 24 inches.

These configuration messages are warnings only. They can often be ignored without undue harm to your system. However, for maximum performance, it is recommended they be strictly followed.

If a warning appears and you choose to ignore it, press any key to continue.

SELECTING HARDWARE MODULES FOR TEST

Once you have verified the module and power configurations, the diagnostics asks you to press any key to proceed. Once this is done the diagnostics format appears and testing begins.

To select a component for testing, move the cursor into the first module icon by pressing the down arrow key on the cursor control pad of the keyboard. The Processor Module icon (always the first module entered) changes to reverse video, if you are using a Monochrome Monitor, or orange, if you are using a Color Monitor. This indicates that the cursor is on it. (All the module icons change to reverse video or orange when the cursor is on them.) To move to the left or right between the icons, use the left and right arrow keys.

Once the cursor is on a module, mark it for testing by pressing MARK. This changes a Monochrome Monitor display from reverse video to bright, and a Color Monitor display from orange to yellow. Pressing CODE-MARK unmarks the module and changes the display back to reverse video or orange, whichever your case may be. In this way you can select and deselect the modules as you choose. The modules are tested in the order that you mark them, and not in any particular order from left to right.

To end most tests at any time, press FINISH and hold momentarily. This removes you from the testing sequence and returns you to the beginning of the diagnostics. At this point you can start the selection process again. Ending the test in this way does not change the current default values.

Up to four individual hard disk and four individual floppy disk modules can be selected for testing. Each module has its own series of questions, prompts, and default values.

The legend at the top of the screen shows the six attribute states for each module: untested, to be tested, cursored, testing, successful, and failed. It also shows the cursor movement keys, and the keys that change the display.

SELECTING SUBMODOLES WITHIN A MODULE FOR TEST

In some cases a module has submodules within it that can be selected and tested without testing the whole module. For example, some Processor Modules have base memory. Memory Expansion Cartridges, RS-232-C ports, RS-422 ports, parallel (printer) I/O's, and timers.

Each of these submodules can be tested without testing any of the others. This allows for very specific diagnostics testing, and saves run time. To select a submodule for testing, move the cursor into the module icon and use the down arrow key to enter the submodule.

When you press the down arrow key, the submodule farthest to the left is displayed in reverse video or orange, in the same way as with the module. The name of the submodule replaces the name of the whole module above the icon. The left and right arrow keys can now be used to move around between the submodules.

Submodules can be selected or deselected by pressing MARK or CODE-MARK in the same way as for the whole module. If submodules are not individually selected, but the entire module is marked, all the tests for that module are run.

When the desired submodules have been marked, return to the module level by pressing the up arrow key. You cannot move from one module to another until the up arrow key has been pressed. With those modules that have no submodules (such as the keyboard), the down arrow and up arrow keys have no function.

INITIAL DIALOGUE

When all the desired modules and submodules have been selected and marked, press GO. This begins the initial dialogue phase.

Each test has a standard sequence of queries and prompts that need to be answered before the test can be run. Each query has a default setting designed to meet the needs of a first-time user. The default is displayed in square brackets immediately after the question. For example:

Stop diagnostic on a memory error? [Y]

In this case the default is Y for yes. The default can be selected by simply pressing RETURN, and going on to the next query. Or you may enter a different response, by typing in another answer, (for example, N for no) and also pressing RETURN.

Most of the queries require a Y or N (yes or no) answer. Some require a word or number, and some require a string of words or numbers.

Whatever value you enter becomes the new default setting, and the diagnostics retains it until it is changed. To restore the original default values for the whole program, rebootstrap the diagnostics according to the instructions in the subsection "Bootstrapping the Diagnostics" above.

Because the default values change according to your selections, the default setting for each query has not been included with the test descriptions in Sections 3 through 9.

NOTE

The diagnostics remembers previous responses to the queries or prompts, so that when a test is run again, the previous answers become the new default settings.

To run the tests again without changing the new default settings, merely press RETURN in answer to each of the queries, without typing in a response.

STARTING THE TESTS

The last prompt that appears in the diagnostics is always the same. It appears only once and comes at the end of all the preliminary dialogues, regardless of how many modules (or submodules) have been selected. It reads:

Enter the number of times to run the diagnostic: [1]

This prompt allows you to choose how many times you want to run the test. If you enter a number larger than 1, the entire test sequence is repeated that many times, without interruption.

However, this does not hold true if you respond with a Y to any "Stop diagnostic on memory error?" query. In this case, the diagnostic stops on the first error it encounters and waits for you to tell it to continue.

When you press RETURN after responding to this final prompt, the tests begin.

VIDEO DISPLAYS DURING AND AFTER THE TESTS

When a test is running with a Monochrome Monitor, the icon is displayed in reverse video. With a Color Monitor the icon is displayed in blue.

A successful test with a Monochrome Monitor causes the icon to remain in reverse video, but changes it to half-bright. A failure causes the icon to blink and to change to a bright reverse video. With the Color Monitor, the test results are shown as green for a successful test, and a bright, blinking red for a failure. These indicators are obvious and persistent and remain until you press FINISH to end the test.

Hard and soft errors are also displayed on the video display while the tests are being run. You see them beneath each module, and they sometimes accumulate if the tests are run a number of times. Soft (or intermittent) errors are displayed in half bright as the left-hand number; hard (or definite) errors are displayed in full bright as the right-hand number. (For example, 5/0 means 5 soft errors and 0 hard errors.)

During testing, the large legend at the top of the screen is replaced by a smaller legend. This legend displays the attribute states, the type of Processor Module being used, the keystrokes used to interrupt the test, and the number of test passes run.

KEYBOARD INTERACTION DURING THE TESTS

During the testing cycle, the diagnostics can be interrupted by pressing, and holding, FINISH. If this is done, the testing ends and the program returns you to the icon menu. Then you can start the tests again.

Exceptions to this interrupt rule are the keyboard and CPU timer tests, which monopolize the data path to the keyboard. Pressing any key during these tests causes the test to show up as a failure.

In most cases, user intervention is not required to run the diagnostics. Once the tests have been chosen and the initial queries and prompts have been answered, the tests run on their own.

However, one exception to this rule is the "Stop diagnostics on a memory error?" query. Answering yes to this question halts the program on the first error. If the program stops, the diagnostics queries you

Continue?

and waits until you type Y (yes) in response. Until a yes answer has been entered, no more tests are run.

3 PROCESSOR MODULES

The following Processor Module tests are not in themselves sufficient to enable troubleshooting of a malfunctioning Processor Module. However, they are sufficient to determine whether the Processor Module is operating correctly.

If an error occurs, see the Processor Manual for your workstation, or contact a field service technician for a more thorough study of the possible problem.

The following components within a Processor Module are generally tested: base memory. Memory Expansion Cartridges, RS-232-C ports, RS-422 ports, parallel (printer) I/O's, and timers.

The upper left corner of your monitor screen displays the type of Processor Module used by your system.

MEMORY EXPANSION CARTRIDGE TESTS

The tests available for the Processor Module's user-accessible Memory Expansion Cartridges are as follows:

- **1st MEM EXP (256 to 512K bytes)**

  This tests the first Memory Expansion Cartridge.

- **2nd MEM EXP (512 to 768K bytes)**

  This tests the second Memory Expansion Cartridge.

- **3rd MEM EXP (768 to 992K bytes)**

  This tests the third Memory Expansion Cartridge. In some Processor Modules only the first two Memory Expansion Cartridges are tested.

When you select the Memory Expansion Cartridge tests, the following two queries (shown below in boldface) appear on the screen:

Stop diagnostic on memory error?

Type Y or N, then press RETURN. If you choose Y for this test, it stops when an error occurs. If N is chosen, the test reports errors but continues testing.

The Memory Expansion Cartridge tests have the following four distinct passes:

- write and read 0's
- write and read 1's
- write address patterns
- read address patterns

If an error occurs (and provided that a yes response was given to the "Stop diagnostic on memory error?" query), the relevant error information is displayed and a question appears:

Continue?

Type Y and press RETURN to continue the test, or type N and RETURN to restart the diagnostics from the icon menu.

The second query is

Do you want to run the Galpat test rather than the standard memory test?

Type Y to run the Galpat test or N to run the standard memory test.

The Galpat (galloping pattern) memory test runs an exhaustive test of the memory. This test can take several hours, depending on the amount of memory to be tested. A sequence of asterisks is displayed during the test to indicate that it is being run. Both parity and invalid data are reported.

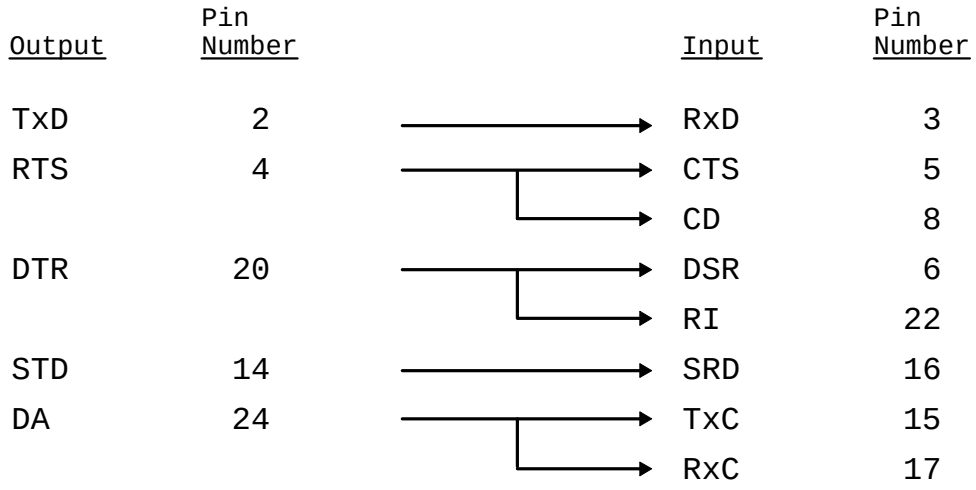
To terminate the memory test at any point, press and momentarily hold FINISH.

RS-232-C TESTS

The RS-232-C tests exercise the RS-232-C interface chip and its supporting logic on the I/O board.

Both RS-232-C ports (A and B) can be tested independently of each other, and each can be tested in several modes of operation. All the combinations of parameters appropriate to each mode are automatically tested.

For the RS-232-C tests to operate properly, each port must be externally looped back to itself. Before running these tests, connect a loopback plug to each port with the following pin arrangements:



These tests and the loopback information presented here also apply to the four RS-232-C ports in the Multiline Port Expander Module.

For further information on loopback connectors, and the RS-232-C interface ports, see the subsection on external interfaces in the Processor Manual for your workstation or the Multiline Port Expander Manual.

When you select the RS-232-C tests the following prompts and queries (shown here in boldface) appear on the screen:

Static status test

The static status test is the first test run when the RS-232-C submodule is selected. It runs automatically, and you are not asked whether it should be run. Its prompt appears on the screen only after the test begins.

The static status test runs several subtests of increasing complexity.

The first subtest checks the interface between the CPU and the RS-232-C interface chip by writing to and reading from the control register inside the interface chip. This subtest determines whether the CPU and the RS-232-C interface chip can successfully communicate with each other.

The second subtest checks the interface between the RS-232-C interface chip and the loopback plug. The following control lines are tested for proper loopback and function:

Name	Function
DTR	Data Terminal Ready
RTS	Request to Send
CTS	Clear to Send
CD	Carrier Detect
DSR	Data Set Ready
RI	Ring Indicator
STD	Secondary Transmit Data
SRD	Secondary Receive Data
DA	Transmit Signal Element Timing
TxC	Transmit Clock
RxC	Receive Clock

The third and final subtest of the static status test checks the same control signals as the second subtest, but does this using interrupts between the CPU and the RS-232-C interface chip.

(When the third subtest executes, nothing is seen on the screen unless an error occurs.)

Do you want to runs:
- Asynchronous mode test?

Type Y to run the test or N to skip over it.

The asynchronous mode test transmits and receives data from the RS-232-C interface chip by passing it through the RS-232-C transmitters, the loop-back, and the RS-232-C receivers, and returning it to the RS-232-C interface chip. The RS-232-C interface chip is initialized to transmit and receive data in asynchronous format.

The transmit data is obtained from a transmit buffer, under interrupts, and the received data is placed into a receive buffer, also under interrupts. After all the data in the transmit buffer has been transmitted and received, the buffers are compared for errors. Any errors detected are displayed on the screen. If other errors are detected during the test, they are displayed when they are detected.

All combinations of baud rates (2400, 4800, 9600, and 19200 baud), data length (5, 6, 7, and 8 bits), parity (none, odd, and even parity), and stop bits (1, 1 1/2, and 2 bits) are tested.

Do you want to run:
- Character sync CRC-16 -test?

Type Y to run the test or N to skip over it.

The character sync CRC-16 test is the same as the asynchronous mode test above, except that the RS-232-C interface chip is initialized to transmit and receive data in bisynchronous format. It uses the CRC-16 cyclical redundancy check (CRC) polynomial.

This test is run at several baud rates (2400, 4800, 9600, and 19,200 baud). The data length is fixed at 8 bits and parity is fixed at none during the execution.

Do you want to run:
- Bit sync data transfer test?

Type Y to run the test or N to skip over it.

The bit sync data transfer test is the same as the asynchronous mode test above, except that the RS-232-C interface chip is initialized to transmit and receive data in synchronous data link control (SDLC) bit synchronization format. It uses the SDLC CRC polynomial.

This test is run at several baud rates (300, 600, 1200, and 2400 baud). The data length is fixed at 8 bits and parity is fixed at none during the execution.

Do you want to run:
?Bit sync abort/idle line test?

Type Y to run the test or N to skip over it.

The bit sync abort/idle line test is the same as the asynchronous mode test above, except that the RS-232-C interface chip is initialized to transmit and receive data in SDLC bit synchronization format. It uses the SDLC CRC polynomial.

This test is run at several baud rates (300, 600, 1200, and 2400 baud). The data length is fixed at 8 bits and parity is fixed at none during the execution. Normal data transmission and reception are tested, as in the bit sync data transfer test.

In addition, generation and recognition of an abort transmission sequence and restarting of the transmission are tested. When the bit sync abort/idle test is running, the message "<<<abort received>>>" appears if the test is successful.

Stop on communications error?

Type Y to stop the test if an error occurs or N to continue. If you type N, any errors that occur are reported as they happen, without stopping the test.

ERROR INFORMATION SCREEN

If the diagnostics detects an error during testing, an error information screen is displayed. This information is divided into the following five sections:

Error Information

This section contains details of the detected error condition. The actual error, as well as the actual and expected test results are displayed.

Probable Causes of the Error

This section lists one to three conditions that may have caused the error. These conditions are by no means the only ones that could occur. However, they do provide a starting point from which to locate the cause of the current error.

RS-232-C Interface Chip (8274) Status Information

This section displays the status of the RS-232-C interface chip channel being tested when the error occurred. The actual and expected state of each bit in the RS-232-C interface chip status registers are given. For a complete description of each bit in the two RS-232-C interface chip status registers, see the Processor Manual for your workstation.

Extended Status Register Information

This section displays the information contained in the Extended Communications status register at the time of the error. The register contains information for both communications channels, but only the information pertaining to the channel being tested is displayed. As in the RS-232-C interface chip status information section above, both the actual and the expected states of each bit at the time of the error are displayed.

Dialogue

This section is where dialogue with the diagnostics program takes place. Requests for continuing or aborting the tests take place in this section.

RS-422 (CLUSTER COMMUNICATIONS) TESTS

The RS-422 tests exercise the cluster communications channel on the I/O board. The loopback for cluster communications in the RS-422 is internal to the interface; therefore there is no loopback connector requirement for these tests.

CAUTION
Running the RS-422 tests while attached to an active cluster damages the cluster lines. Disconnect your workstation from the cluster before running these tests.

When the RS-422 tests are selected, the following four queries (shown here in boldface) appear on the screen:

Do you want to run
- Cluster maintenance mode test?

Type Y to run the test or N to skip over it.

The cluster maintenance mode test loops back a number of communications test frames and checks for timeout, CRC, overrun, data, channel hold, and other errors. When the test completes, all errors are reported.

The next query on the screen is prefaced by a requirement:

The next test requires that two workstations be taken off the cluster master and connected to each other via a cluster cable.

Do you want to run:
- Interprocessor data transfer test?

Type Y to run the test or N to skip over it.

The interprocessor data transfer test performs transfers between two workstations, using DMA for transmission and reception. For proper operation, both workstations must be running this test simultaneously and be connected together by a standard cluster communications cable. However, they must not be connected to an operational cluster when you are running this test.

Stop on a communications error?

Type Y to stop the test on an error or N to continue the test even if an error occurs.

Fast cluster communication?

Type Y to execute the tests at 1.8 megabaud or N to execute the tests at the standard cluster speed of 307 kilobaud.

PARALLEL I/O (PRINTER) TESTS

The parallel I/O (printer) tests check the parallel printer port and its supporting logic. This test can be exercised with or without the use of interrupts.

When you select the parallel I/O (printer) tests, the following four queries (shown here in boldface) appear on the screen:

Do you want to run:
- Barber pole test (without, interrupts)?

Type Y to run the test or N to skip over it.

The barber pole test (without interrupts) outputs one page (66 lines, 132 columns) of a test pattern consisting of all 96 printable ASCII characters. Each successive line is shifted one character to the left, resulting in a "barber pole" pattern.

Before the test pattern is transmitted, the status of the printer is checked. If the printer or the print buffer is busy or not selected, an error occurs and the test is suspended. However, if the printer status is positive, the diagnostics transmits the test pattern. It then polls the printer status after each character is transmitted. If the print buffer does not free itself to accept another character before the maximum wait time (see below), an error occurs and the test is suspended.

Do you want to run:
- Barber pole test (with interrupts)?

Type Y to run the test or N to skip over it.

This test is identical to the barber pole test (without interrupts), except that it does not poll the printer status after each character is transmitted. Instead, the test waits for an interrupt to be generated by the printer acknowledge line, signaling that the printer is ready to receive another character.

If the interrupt is not generated before the maximum wait time (see below), or the printer status shows that the printer is still busy after the interrupt, an error occurs and the test is suspended.

Max printer wait time (ms)?

This is the maximum length of time (in milliseconds) the diagnostics will wait for a response from the printer before it ends the test.

Enter a number in milliseconds. The number you type in depends on several factors, such as the speed of the printer and the size of the character buffer. For more information about your individual printer, see the manual provided with your printer system.

Bypass any errors & continue with diagnostics?

If you select Y and the parallel I/O (printer) tests fail, the test stops and displays the printer error messages.

If you choose N and the test fails, the test displays the error messages, but continues to run indefinitely until it is stopped by pressing FINISH.

PRINTER ERROR MESSAGES

Once an error has occurred, and an error message has been displayed, testing is suspended. There are two portions to an error message: the error message itself and the printer status.

The error message section is a brief explanation of the type of error that occurred. For example, >>> Timeout waiting for printer interrupt <<<.

The printer status section shows the status of the printer port at the time of the error.

BASE MEMORY TEST

The base memory test is almost identical to the Memory Expansion Cartridge tests described above, except that it tests the resident base memory in the Processor Module. During this test, the diagnostics relocates itself to the first Memory Expansion Cartridge and then writes to and reads from the base memory using a slightly different pattern. This test uses all the same passes used by the Memory Expansion Cartridge tests.

To run this test, your system must have at least one Memory Expansion Cartridge. Without this the test fails and an error message is displayed.

CPU TIMER TEST

When selected, this test sets time intervals between 100 and 800 milliseconds, in 100-millisecond increments, to verify the operation of the CPU timer.

You must have a keyboard connected to your workstation to run this test. Pressing any key on the keyboard during this test causes the test to fail.

VIDEO CONTROLLER TEST

The video controller diagnostics checks the video RAM, the font RAM, and the video logic of the Processor Module. It reports all errors found, unless you answer N to the "List all errors found?" query.

The video controller test also serves as a user-verifiable, non-self-checking visual test for the proper operation of the Monochrome Monitor. Choosing this submodule runs exactly the same test as choosing the Monochrome Monitor icon. To stop any of these tests for closer inspection, press PREV PAGE. To restart the tests, press NEXT PAGE.

The video attribute test, font display test, and mosquito net test are repeated four times, each time with a different intensity and background. The video memory test and cursored string test run only once.

The sequence of the five video controller tests is as follows.

VIDEO MEMORY TEST

The video memory test runs in two phases.

In the first phase, the diagnostics shows a representative set of module icons and then scrolls them upward. This tests the video RAM.

In the second phase, the diagnostics fills the screen with different characters and cycles through them, testing the font RAM.

At the end of both cycles the display returns to its original state, having exercised all of the video memory.

VIDEO ATTRIBUTE TEST

The video attribute test displays all the video attributes on the screen (for example, half-bright, bold, struck-through, underlined).

FONT DISPLAY TEST

The font display test shows the character font used by the diagnostics. This is not the standard workstation font, but instead, a special font designed to test all the font capabilities in the video memory.

MOSQUITO NET TEST

The mosquito net test displays a screenful of one-pixel-thick lines used to test line clarity and pincushion distortion.

CURSORED STRING TEST

The cursored string test fills the screen with text and moves the cursor to each "T" in the text, in turn.

When all the tests have been run, the memory errors are displayed. (This assumes-a Y answer to the "List all errors found?" query.) If an N answer was given or no errors are found, the diagnostics returns to the icon menu ready to run more tests.

4 MULTILINE PORT EXPANDER MODULE TESTS

5 DISK MODULES

DUAL FLOPPY DISK MODULE

INTRODUCTION

The following Dual Floppy Disk Module tests are not in themselves sufficient to enable troubleshooting of a malfunctioning Dual Floppy Disk Module. However, they are sufficient to determine whether the Dual Floppy Disk Module is operating correctly.

If an error occurs, refer to the Dual Floppy Disk Manual or contact a field service technician for a more thorough study of the possible problem.

> CAUTION
>
> The Dual Floppy Disk Module tests destroy the data on the disks in the floppy disk drives. Before running any of these tests, remove the diagnostics disk, and replace it with a scratch disk.

FLOPPY DISK TESTS

When you select the floppy disk diagnostics, the following questions (shown here in boldface) appear on the screen:

Stop diagnostic on a disk error?

Type Y to stop the test on an error, or N to continue the test. Errors are registered and displayed even if you do not choose to stop.

Run quick verification? (some of the tests will destroy data)

Type Y to run a quick verification (recalibrate and format/verify only) or N to run the full verification.

Typing N also allows you to customize your test runs by individually selecting diagnostic tests. (For more information, see below under "Run full verification?")

A quick verification recalibrates the read/write head (returns it to track 00), formats the floppy disk, and then reads back the format to make sure it was correctly written. These tests are described below under "Recalibrate test" and "Format with verify."

Run full verification? (some of the tests will destroy data)

Type Y to run a full verification (all tests) or N to customize the diagnostics by selecting individual tests. (This occurs only if N was answered to "Run quick verification?")

If you respond with N you can select specific tests to be run. These tests are described below in the subsection "Individual Test Selection."

If individual tests are selected, the following questions are still asked. However, they are asked later, after the individual test selection is complete.

If you respond to "Run full verification?" with Y, the next question is

Change detail parameters?

The detail parameters are characteristics of the floppy disk format. Responding to this question with Y allows you to alter the format.

If you choose Y, the following queries appear on the screen:

Number of retries?

The number of retries refers to the number of times the diagnostics tries to read data from a sector on the floppy disk. Several retries are generally chosen. Type in the number of retries you desire.

Number of bytes per sector?
Number of sectors per track?
Number of tracks per cylinder?
Number of cylinders per disk?

These parameters specify the number and size of the data areas on the floppy disk. Enter the appropriate numbers or use the default settings.

The bytes per sector must be either 128, 256, 512, or 1024.

Debug?

Type Y to use the Debugger or N to skip over it. If you choose Y and a disk error occurs, the diagnostics asks

Enter the debugger?

Type Y to enter the Debugger or N to continue with the diagnostics. If you enter the Debugger by mistake, press GO. This returns you to the diagnostics exactly where you were before.

If you choose N in answer to "Debug?" the next question is

Show activity (dots)?

Type Y to show dots on the screen when sectors or tracks are written to or read from the floppy disk drive. Type N to skip over the activity dots.

Filler data?

Enter a four-digit hexadecimal number to change the data pattern written to the floppy disk drive. The default [6DB6] is a worst case pattern, maximizing the testing value of the diagnostics. It causes the greatest amount of response from the floppy disk drive during the write/read process.

After answering the "Filler data" question, if you answered Y to "Run quick verification?" or "Run full verification?", the diagnostics prompts you to

Enter the number of times to run the diagnostic

Once you respond, the tests are run.

SELECTING INDIVIDUAL TESTS

If you answered N to "Run quick verification?" and "Run full verification?", you are now able to individually select the tests you wish to run. These are asked immediately after the "Run full verification?" question.

You can choose from the following tests:

Recalibrate test

Type Y to run the test or N to skip over it.

The recalibrate test checks the basic functioning of the read/write head positioning mechanism and track 00 sensor.

This test first initializes the floppy disk interface and issues a recalibrate command to the floppy disk controller. It then issues a command to step the head inward to the center of the disk. It ends by issuing another recalibrate command and stepping the head back to track 00.

Any errors detected during recalibration are displayed.

Sequential seek test

Type Y to run the test or N to skip over it.

The sequential seek test checks the function of the head positioning mechanism by stepping the head from track 00 to the innermost track on the disk, one track at a time.

Any errors detected during sequential seek are displayed.

Random seek test

Type Y to run the test or N to skip over it.

The random seek test checks the function of the head positioning mechanism by stepping the head from track TPD/2 to track TPD/2-1 to track TPD/2+1 to track TPD/2-2 to track TPD/2+2, and so on. (TPD represents the number of tracks per floppy disk.)

Any errors detected during random seek are displayed.

Format with verify (destructive)

Type Y to run the test or N to skip over it.

The format with verify test formats a floppy disk (or disks if both drives were selected). The disks are formatted one track at a time. Data is first written to the disk, then read back.

Sequential write/read single sectors (destructive)

Type Y to run the test or N to skip over it.

The sequential write/read single sectors test writes data to each sector on a track, one sector at a time.

First, the odd-numbered, logical sectors are written with filler data. Next, the even-numbered, logical sectors are written, using the ones complement of the filler data. After all the sectors on the track are written, the data in each sector is verified against the data written. The test is repeated on three tracks: track 00, track TPD/2, and track TPD-1.

Random write/read single sectors (destructive)

Type Y to run the test or N to skip over it.

The random write/read single sectors test performs a write and a read of a random number of sectors on each tested track.

All tracks are tested from track TPD/2 to track TPD/2-1 to track TPD/2+1 to track TPD/2-2 to track TPD/2+2, and so on.

Sequential write/read multiple sectors (destructive)

Type Y to run the test or N to skip over it.

The sequential write/read multiple sectors test writes data to each sector on a track, one half track at a time.

First, sectors 1 to SPT/2 are written using a ramp pattern (0123456789). Then sectors SPT/2+1 to SPT are written. The data in each sector is then verified against the data written. (SPT is the number of sectors per track on the disk.)

Function - read track format

Type Y to use this function or N to skip over it.

The read track format function reads an entire track into the DMA buffer and displays it 256 bytes at a time.

The function prompts for a cylinder number and a head number. Press RETURN in response to the cylinder number prompt to exit the function. Invalid entries are reported with a beep. If this happens, backspace and enter the numbers again.

Once the first 256 bytes in the buffer are displayed, the function then asks "More?"

Type Y to display the next 256 bytes in the buffer. Type N to read another track.

Function - display/modify sector

Type Y to use this function or N to skip over it.

The display/modify sector function allows you to display and, optionally, modify any sector on the floppy disk under test.

The function prompts for a cylinder number, a sector number, and a head number. Invalid entries are reported with a beep. If this happens, backspace and enter the numbers again.

This test is interactive, and while it is running you are asked to respond to several more questions and prompts.

Enter a cylinder number in response to the **cylinder**: prompt. If you want to discontinue, pressing RETURN at this point terminates the display/modify sector function.

If you want to continue, enter the appropriate numbers when the **head number**: and **sector number**: prompts appear.

The sector specified is then read into the DMA buffer, and the first 256 bytes are displayed.

The function then" asks "**More?**" Type Y to display the next 256 bytes in the buffer. Type N to modify the sector or inspect another sector.

The function asks "**Modify?**" Type Y to modify the sector. Type N to inspect another sector.

The function asks "**Byte?**" Enter the decimal number of the byte to be modified.

The function then displays the byte number and its hexadecimal value. Type a new hexadecimal value to change the byte, or press RETURN to leave the byte unchanged.

After the sector has been modified, you are asked "**Write sector?**" Type Y to rewrite the sector on the floppy disk with the modified data. Type N to leave the modified sector unchanged.

Function - copy drive to drive

Type Y to use this function or N to skip over it.

The copy drive to drive function copies the entire contents from one floppy disk to another.

During the selection process the entire dual floppy disk icon must be marked. The diagnostics then assumes that the source and destination drives are F0 to Fl, respectively.

The destination floppy disk must be formatted using the format with verify test (see above) before it can be used to copy from drive to drive. After each track is written to the destination disk, it is verified against the data on the source disk.

Function - read disk address

Type Y to use this function or N to skip over it.

The read disk address function reads the identification field of the next sector to pass under the read/write head.

This function prompts you for the cylinder number and the head number.

Function - loop on track format (destructive)

Type Y to use this function or N to skip over it.

The loop on track format function continuously formats one track on the disk.

This function asks you for the cylinder number and the head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

Function - loop on sector read

Type Y to use this function or N to skip over it.

The loop on sector read function continuously reads one track on the disk.

This function prompts you for the cylinder number and the head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

Function - loop on sector write (destructive)

Type Y to use this function or N to skip over it.

The loop on sector write function continuously writes one track on the disk.

This function prompts you for the cylinder number and the head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

Function - compare drive to drive

Type Y to use this function or N to skip over it.

The compare drive to drive function compares the data on two floppy disks. It is the same as the verification function of the copy drive to drive function described above.

Function - read sequential tracks

Type Y to use this function or N to skip over it.

This function reads the entire floppy disk, one track at a time.

Function - loop on full track read

Type Y to use this function or N to skip over it.

The loop on full track read function continuously reads a full track of the disk.

This function prompts you for the cylinder number and head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

ERROR MESSAGE FORMAT

When an error is detected during the floppy disk diagnostics, a brief description of the error condition is displayed on the screen. This is followed by the status of the floppy disk controller. The status information includes any or all of the following:

- The most recently executed floppy disk controller command. This command is displayed as a hexadecimal byte and a written message.

- The contents of the working status register of the floppy disk controller, as of the most recent command.

- The residual byte count from the last DMA transfer.

- The cumulative number of soft errors that have occurred during the execution of the current tests. These errors accumulate over all tests and all passes, for both drives. They are displayed underneath the module icon in the bottom window as they occur.

  Soft errors are errors that occur intermittently. They do not necessarily take place every time the diagnostics is run. Often they are recoverable, if the tests are run again. Soft errors are displayed in half-bright on the left side of the slashed number below the module icon. (For example, 8/0 means eight soft errors, zero hard errors.)

- The cumulative number of hard errors that have occurred during the execution of the current tests. These are shown underneath the module icon in the bottom window as they occur.

  Hard errors indicate a failure of some portion of the hardware inside a module or submodule. They are generally not recoverable, even if the tests are run again. Hard errors are displayed in full-bright on the right side of the slashed number below the module icon. (For example, 0/5 means zero soft errors, five hard errors).

The interpretation of the bytes displayed in the error message format above can be found in tables listing the controller flag, controller command, and status register summaries in the Dual Floppy Disk Manual.

FLOPPY/HARD DISK MODULE

INTRODUCTION

The following Floppy/Hard Disk Module tests are not in themselves sufficient to enable troubleshooting of a malfunctioning Floppy/Hard Disk Module. However, they are sufficient to permit you to determine whether the Floppy/Hard Disk Module is operating correctly.

If an error occurs, refer to the Floppy/Hard Disk Manual, or contact a field service technician for a more thorough study of the possible problem.

FLOPPY DISK TESTS

The diagnostic questions for the floppy disk drive in the Floppy/Hard Disk Module are exactly the same as those for the floppy disk drives in the Dual Floppy Disk Module. For reference to those tests, see the "Floppy Disk Tests" subsection above.

CAUTION

The Floppy/Hard Disk Module tests destroy the data on the disks under test.

Remove the diagnostics disk from the floppy disk drive and back up the data on the hard disk before running any of these tests. A scratch disk should be inserted in the floppy disk drive in place of the diagnostics.

HARD DISK TESTS

When you select the hard disk diagnostics, the following prompts (shown here in boldface) appear on the screen:

Enter Drive Vendor Code

The drive vendor code appears as a circled letter on the bottom of the chassis of all Floppy/Hard and Hard Disk Modules, next to the bad spot information. The drive vendor code determines the drive parameters used by the diagnostics to access the hard disk. It does not apply to floppy disk modules.

If the vendor code on the bottom of your disk drive is A or B, you do not have to enter the letter. A and B are the default values, and therefore need not be entered.

If the vendor code is any letter other than A or B, enter that letter after the prompt.

If no vendor code is specified on the module bottom, the number of cylinders and heads must be entered. These are entered after answering Y to "Change detail parameters?"

If the number of cylinders and heads is not on the label underneath the module, they can be obtained from one of the OEM disk drive appendixes in the Hard Disk Upgrades and Expansions Manual.

For further information about vendor codes, see the current Release Notice accompanying the diagnostics.

CAUTION

If your drive vendor code is not A or B and you do not enter the correct vendor code letter, the hard disk is formatted according to the default values. This can prevent the proper operation of the diagnostics.

After the drive vendor code information is entered, the diagnostics asks:

Stop diagnostic on disk error?

Type Y to stop the test on an error or N to continue the test, regardless of an error.

Run quick verification? (some of the tests will destroy data)

Type Y to run a quick verification (recalibrate, sequential seek, format disk, and random write/read single sectors tests) or N to run the full verification.

Typing N also allows you to customize your test runs by individually selecting diagnostic tests. (For more information, see below under "Run full verification?")

A quick verification recalibrates the read/write head (returns it to track 00), tests the read/write head mechanism, formats the hard disk, and randomly selects tracks to write to. It then reads back the data to make sure it was written correctly. For further information, see below under "Recalibrate test," "Sequential seek test," "Format disk," and "Random write/read single sectors."

Run full verification? (some of the tests will destroy data)

Type Y to run a full verification (all tests) or N to customize the diagnostics by selecting individual tests. (This occurs only if N was answered to "Run quick verification?")

If you respond with N, you can select specific tests to be run. These tests are described below in the subsection "Individual Test Selection."

If individual tests are selected, the following questions are still asked. However, they are asked later, after the individual test selection is complete.

If you respond to "Run full verification?" with Y, the next question is

Change detail parameters?

The detail parameters are the characteristics of the hard disk format. Responding to this question with Y allows you to alter the format.

If you choose Y, the following queries appear on the screen:

Number of retries?

The number of retries refers to the number of times the diagnostics tries to read data from a sector on the hard disk. Several retries are generally chosen. Type in the number of retries you desire.

Number of bytes per sector?
Number of sectors per track?
Number of tracks per cylinder?
Number of cylinders per disk?

These parameters specify the number and size of the data areas on the hard disk. Enter the appropriate numbers or use the default settings. The controller only supports byte per sector sizes of 128, 256, 512, or 1024.

Stepper rate?

This parameter determines the rate at which the read/write head on the hard disk drive steps from track to track. Type in a number for the stepper rate or use the default settings. See the Floppy/Hard Disk Manual for more details on the stepper rate.

Debug?

Type Y to use the Debugger or N to skip over it. If you choose Y, and a disk error occurs, the diagnostics asks

Enter the debugger?

Type Y to enter the Debugger or N to continue with the diagnostics. If you enter the Debugger by mistake, press GO. This returns you to the diagnostics exactly where you were before.

If you choose N in answer to "Debug?" the next question is

Show activity (dots)?

Type Y to show dots on the screen when sectors or tracks are written to or read from the hard disk drive. Type N to skip over the activity dots.

Filler data?

Enter a four-digit hexadecimal number to change the data pattern written to the hard disk drive. The default [6DB6] is a worst-case pattern, maximizing the testing value of the diagnostics. It causes the greatest amount of response from the hard disk drive during the write/read process.

Enter bad spot data

The hard disk diagnostics test all sectors on the disk. Normally, the diagnostics stops testing when a defect is encountered. However, the diagnostics does not stop if the defect is contained in a known bad spot.

The bad spot data appears on the bottom of your Hard Disk Module, next to the vendor code. It says "cylinder/head/BFI," and gives a list of the known defect information for the hard drive. BFI stands for "bytes from index" and is commonly referred to as an "offset" or an "offset from index." This information should be recorded when you first receive the module.

If your disk drive contains bad spots, you enter the bad spot data after the following prompt:

No mapped defects have been previously entered

Enter the bad spot information in this format:

cyl/head/bfi	(for example, 250/2/1234)
cyl/head/#sector	(for example, 250/2/#2)

You can enter several defect parameters per line, separated by a space, or you can enter each one on a new line. Press RETURN when you have finished entering the bad spot data.

If no bad spots exist, the vendor code label says "no media defects." In this case, press RETURN without entering any information after the prompt.

When the diagnostics detects a defect in a known bad spot, it displays the following message:

Mapped defect at cylinder: nnn head: nnn sector: nnn

For further information about bad spot data, see the current Release Notice accompanying the diagnostics.

After responding to the "Enter bad spot data" prompt, if you answered Y to "Run quick verification?" or "Run full verification?" the diagnostics prompts you to

Enter the number of times to run the diagnostic

Once you respond, the tests are run.

SELECTING INDIVIDUAL TESTS

If you answered N to "Run quick verification?" and "Run full verification?" above, you are now able to individually select the tests you wish to run. These are asked immediately after the "Run full verification?" question.

You can choose from the following tests:

Recalibrate test

Type Y to run the test or N to skip over it.

The recalibrate test checks the basic functioning of the read/write head positioning mechanism.

This test issues a recalibrate command to the disk controller, followed by a seek command, which moves the read/write head to the last cylinder on the disk under test.

Any errors detected during recalibration are displayed.

Sequential seek test

Type Y to run the test or N to skip over it.

The sequential seek test checks the function of the head positioning mechanism by stepping the head from track 00 to the innermost track on the disk, one track at a time.

Any errors detected during sequential seek are displayed.

Format disk (destructive)

Type Y to run the test or N to skip over it.

The format disk test formats the hard disk (or disks, if both drives are selected). The disks are formatted one track at a time.

Random seek test with ID scan

Type Y to run the test or N to skip over it.

The random seek test with ID scan checks the function of the head positioning mechanism by stepping the head from cylinder CPD/2 to cylinder CPD/2-1 to cylinder CPD/2+1 to cylinder CPD/2-2 to cylinder CPD/2+2, and so on. (CPD represents the number of cylinders per hard disk.)

This test also reads the identification areas of the sectors.

Any errors detected during random seek are displayed.

Write/read all tracks (destructive)

Type Y to run the test or N to skip over it.

The write/read all tracks test sequentially writes a ramp pattern (0123456789) to every track on the disk under test. The test then reads the data back to verify that it was correctly written.

Sequential write/read single sectors (destructive)

Type Y to run the test or N to skip over it.

The sequential write/read single sectors test writes data to each sector on a track, one sector at a time.

First, the odd-numbered, logical sectors are written using a ramp pattern (0123456789). Next, the even-numbered, logical sectors are written, using the ones complement of the ramp pattern. After all the sectors on the track are written, the data in each sector is verified against the data written. The test is repeated on three cylinders: cylinder 00, cylinder CPD/2, and cylinder CPD-1.

Random write/read single sectors (destructive)

Type Y to run the test or N to skip over it.

The random write/read single sectors test performs a write/read of a random number of sectors on each tested track.

All tracks in each cylinder are tested. All cylinders are tested from cylinder CPD/2 to cylinder CPD/2-1 to cylinder CPD/2+1 to cylinder CPD/2-2 to cylinder CPD/2+2, and so on.

Sequential write/read multiple sectors (destructive)

Type Y to run the test or N to skip over it.

The sequential write/read multiple sectors test writes data to each sector on a track, one-half track at a time.

First, sectors 1 to SPT/2 are written using a ramp pattern (0123456789). Then sectors SPT/2+1 to SPT are written. The data in each sector is then verified against the data written.

(SPT is the number of sectors per track on the hard disk.) All the cylinders of the hard disk are tested.

Function - display/modify sector

Type Y to use this function or N to skip over it.

The display/modify sector function allows you to display and, optionally, modify any sector on the hard disk under test.

The function prompts for a cylinder number, a sector number, and a head number. Invalid entries are reported with a beep. If this happens, backspace and enter the numbers again.

This test is interactive, and while it is running you are asked to respond to several more questions and prompts.

Enter a cylinder number in response to the **cylinder**: prompt. If you want to discontinue, pressing RETURN at this point terminates the display/modify sector function.

If you want to continue, enter the appropriate numbers when the **head number**: and **sector number**: prompts appear.

The sector specified is then read into the DMA buffer, and the first 256 bytes are displayed.

The function then asks "**More?**" Type Y to display the next 256 bytes in the buffer. Type N to modify the sector or inspect another sector.

The function asks "**Modify?**" Type Y to modify the sector. Type N inspect another sector.

The function asks "**Byte?**" Enter the decimal number of the byte to be modified.

The function then displays the byte number and its hexadecimal value. Type a new hexadecimal value to change the byte, or press RETURN to leave the byte unchanged.

After the sector has been modified, you are asked "**Write sector?**" Type Y to rewrite the sector on the hard disk with the modified data. Type N to leave the modified sector unchanged.

Function - read boot ROM

Type Y to use this function or N to skip over it.

The read boot ROM function reads and displays the contents of the Floppy/Hard Disk Module's bootstrap ROM.

Function - loop on track format (destructive)

Type Y to use this function or N to skip over it.

The loop on track format function continuously formats one track on the disk.

This function asks you for the cylinder number and the head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

Function - loop on sector read

Type Y to use this function or N to skip over it.

The loop on sector read function continuously reads one track on the disk.

This function prompts you for the cylinder number and the head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

Function - loop on sector write (destructive)

Type Y to use this function or N to skip over it.

The loop on sector write function continuously writes one track on the disk.

This function prompts you for the cylinder number and the head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

Function - read sequential tracks

Type Y to use this function or N to skip over it.

This function reads the entire hard disk, one track at a time.

Function - loop on full track read

Type Y to use this function or N to skip over it.

The loop on full track read function continuously reads a full track of the disk.

This function prompts you for the cylinder number and head number. It is designed to support troubleshooting using test equipment and runs until you press FINISH.

ERROR MESSAGE FORMAT

When an error is detected during the hard disk diagnostics, a brief description of the error condition is displayed on the screen. This is followed by the status of the hard disk controller. The status information includes any or all of the following:

- The most recently executed hard disk controller command. This command is displayed as a hexadecimal byte and a written message.

- The contents of the status and error registers of the hard disk controller, as of the most recent command.

- The residual byte count from the last DMA transfer.

- The cumulative number of soft errors that have occurred during the execution of the current tests. These errors accumulate over all tests and all passes, for both drives. They are displayed underneath the module icon in the bottom window as they occur.

  Soft errors are errors that occur intermittently. They do not necessarily take place every time the diagnostics is run. Often they are recoverable, if the tests are run again. Soft errors are displayed in half-bright on the left side of the slashed number below the module icon. (For example, 8/0 means eight soft errors, zero hard errors.)

- The cumulative number of hard errors that have occurred during the execution of the current tests. These are shown underneath the module icon in the bottom window as they occur.

  Hard errors indicate a failure of some portion of the hardware inside a module or submodule. They are generally not recoverable, even if the tests are run again. Hard errors are displayed in full-bright on the right side of the slashed number below the module icon. (For example, 0/5 means zero soft errors, five hard errors.)

The interpretation of the bytes displayed in the error message format above can be found in tables listing the controller flag, controller command, and status register summaries in the Floppy/Hard Disk Manual.

DISK UPGRADE AND DISK EXPANSION MODULES TESTS

The tests used for the hard disks in the Disk Upgrade and Disk Expansion Modules are the same as those described in the "Hard Disk Tests" subsection above.

Note, however, that the vendor code of the Disk Expansion and Disk Upgrade Modules may differ from the vendor code of the modules to which they are attached.

For further information on the Disk Upgrade and Disk Expansion Modules, see the Hard Disk Upgrades and Expansions Manual.

6 MONITORS

MONOCHROME MONITOR TESTS

The Monochrome Monitor tests are exactly the same tests as those run by the Video Controller in the Processor Module. Selecting either the Video Controller submodule or the Monochrome Monitor icon produces the same results. In either case, close visual inspection of the Monochrome Monitor is required to verify its proper operation.

Tests for the Graphics Controller Module can also be run on the Monochrome Monitor. In order to do this, the Monochrome Monitor must be cabled directly to the Graphics Controller Module. The Graphics Controller Module tests appear in monochrome green.

Not all the Graphics Controller Module tests are run with the Monochrome Monitor. The tests you will see are

- graphics control register 1
- graphics control register 2
- memory test
- line drawing test 1: concentric rectangles
- overlapping lines test
- pattern and vector mode test

For further information about your Monochrome Monitor, or for help diagnosing a problem, see the Monochrome Monitor Manual, or consult a field service technician familiar with your system.

COLOR MONITOR TESTS

The diagnostic tests for the Color Monitor require no interaction, but do require that you pay close attention to the screen when the tests are being run. Since these tests are not self-checking, it is up to you to verify their accuracy for yourself.

If the Processor's video controller submodule tests are run with the Color Monitor, the tests appear as a monochrome display. This is normal, and does not indicate any problem with the Color Monitor.

For further information, see the "Video Controller Test" subsection in Section 3, "Processor Modules."

The Color Monitor tests cannot be run with a Monochrome Monitor attached to your workstation.

When the Color Monitor is marked during the selection process and you press RETURN, the diagnostics queries you only twice:

Delay? (1-10)

This question allows you to speed up or slow down the pace at which the tests are run. The default setting is 10, the slowest setting. If you choose 1, the fastest setting, the tests run very rapidly. However, you can stop the screen by pressing PREV PAGE, and restart it by pressing NEXT PAGE. The speed you choose becomes the new default setting until it is changed.

Provide labels?

This question allows you to suppress verbal descriptions of each test from the screen. Since the Color Monitor tests are not self-checking, labels are provided to help you verify what you see. The default on this question is Y, so you must type in N to suppress the labels. Once suppressed, this becomes the new default setting until it is changed.

The following tests are run when the Color Monitor is selected.

COLOR BAR TEST 1

This test presents a block of color divided in half, each side showing three variations of the same color. The left half is three shades of red, and the right half is three shades of green. They are all arranged in vertical bars. From left to right you should see

- low red
- medium red
- full red
- low green
- medium green
- full green

This color bar test is a visual test only. Relative approximations of the three shades of each color are sufficient to prove that the Color Monitor works. There is no confirmation of the success or failure of this test from the diagnostics.

COLOR BAR TEST 2

This test also presents a block of color divided in half, showing three variations of the same color on each side. The left side has three shades of blue, and the right side has three shades of white.

Technically, the colors of the right half are considered white by the workstation, but visually they will appear to you as three shades of gray. This is normal and does not represent any failure of the Color Monitor or the diagnostics. From left to right you should see

- low blue
- medium blue
- full blue
- low white
- medium white
- full white

This color bar test is a visual test only. Relative approximations of the three shades of each color are sufficient to prove that the Color Monitor works. There is no confirmation of the success or failure of this test from the diagnostics.

SPEAKER TEST

This test checks the speaker in the Color Monitor. It sounds for approximately one second.

7 GRAPHICS CONTROLLER MODULE

8 TELEPHONE MANAGER MODULE

9 KEYBOARD

INTRODUCTION

The following keyboard tests are not in themselves sufficient to enable troubleshooting of a malfunctioning keyboard. However, they are sufficient to determine if the keyboard is functioning correctly.

If an error occurs, refer to the Keyboard Manual or contact a field service technician for a more thorough study of the possible problem.

KEYBOARD TESTS

When the keyboard icon is selected, the following queries and prompts (shown here in boldface) appear on the screen.

Do you want to run the keyboard echo test?

The keyboard echo test checks the circuitry that signals the workstation when a keyboard key is pressed. A picture of the keyboard appears on the screen during execution of this test. When keys on the keyboard are pressed, the corresponding key area lights up on the screen. The keyboard LEDs also light up when the appropriate keys are pressed. This test can be used to locate malfunctioning keys and inoperative keyboard LED indicators.

Type Y to run the keyboard echo test or N to skip over it.

If you choose Y, press both ACTION and FINISH together to exit the screen. Exiting the screen returns you to the beginning of the keyboard test, ready to run again.

The keyboard echo test is the first question asked and the last test executed in the keyboard diagnostics.

Stop diagnostics on keyboard error?

Type Y to stop on an error or N to continue if an error occurs. If you choose N, hard and soft errors are displayed below the module icon as they occur.

Display all hex codes that come from the keyboard?
(must reset to exit)

Type Y to display the keyboard hexadecimal codes or N to run the keyboard diagnostics in the conventional (nonhexadecimal) manner.

If you answer Y to this question, any key pressed on the keyboard is accompanied by its hexadecimal code on the screen.

> NOTE
>
> To exit this test, it is necessary to reboot-strap the diagnostics. Reinsert the diagnostics disk in the floppy disk drive and press the reset button on the back of the Processor Module.

When the keyboard diagnostics begins, several short subtests (shown in boldface below) are executed. If no errors are found after each subtest, the message "OK" is displayed on the screen.

I-BUS HARDWARE RESET

The I-Bus hardware reset test checks the software-controlled hardware reset of the keyboard. This reset causes the keyboard to turn on all its LED indicators.

The next four tests are subtests of the I-Bus hardware reset test.

ID Sequence

The ID sequence subtest checks to see if the keyboard can identify itself to the Processor Module.

KBD Software Reset:

The KBD software reset subtest checks the keyboard's ability to execute a soft reset command.

The KBD software reset command is the first communication received by the keyboard from the Processor Module. Therefore, it is at this point that the keyboard "learns" which of its ports are connected to that module. (The keyboard has two ports, at its right and left corners, either of which can be used to connect the keyboard to the video monitor base, and thus to the Processor Module.) Upon successful receipt of this command, the keyboard turns off its LED indicators.

ROM Checksum

The ROM checksum subtest performs a checksum of the ROM in the keyboard microcontroller. The diagnostics is expecting the result to be the hexadecimal 0F0h. Any redesign of the keyboard firmware is required to ensure a ROM checksum of 0F0h.

Loopback Test

The loopback test checks the bidirectional serial communications channel between the Processor Module and the keyboard microcontroller. Do not press any key during this test or the test will fail.

After these subtests are executed, the diagnostics tests the second port on the keyboard. It is looking for a pointing device or other attached accessory. The following status message appears on the screen:

Switching to I-Bus Position 02

No device should be attached to the I-Bus Position 02. If anything is attached, the test fails and a message on the screen says

Wrong ID code

An error message is also displayed.

Detach the device at I-Bus Position 02 and run the test again.

If a second device is not present at I-Bus Position 02, another status message appears:

No device attached

At this point, the keyboard diagnostic ends, and you are returned to the icon menu.

APPENDIX A: DIAGNOSTICS SELECTION PROGRAM (SP)

The Selection Program (SP) is an application program that allows you to preconfigure the diagnostics for a particular purpose. You may want to run a battery of tests without having to intervene, or you may want to use only one or two features.

SP enables you to put together a custom diagnostics that can be bootstrapped exactly like the standard software.

SP can be used to

- Change the default responses to diagnostic prompts, so that the most frequently used responses can be selected by simply pressing RETURN.

- Completely suppress some or all diagnostic queries, so that the default values you specify will always be used. The tests can then be run without your input.

- Replace the normal module selection process with a preselection program arranged by module type. In this way, the preconfigured diagnostics tests any number of preselected modules, without requiring you to mark them for testing.

INSTALLING SP

To install SP, refer to the installation instructions in the current Release Notice of the diagnostics.

RUNNING SP

To run SP, type the command "Diagnostics Selection Program" (or an abbreviation such as "D S P") in the command field.

SP INPUT AND OUTPUT FILES

SP asks you to specify both input and output files. The default for the input file is [sys]<sys>CP.run, the standard diagnostic. The output file, which you must specify, is the custom diagnostics generated by SP. SP does not modify the input file in any way.

SP OPTIONS

SP then displays the following questions:

Do you want the custom diagnostic to:

Pause for power configuration check?
Stop on a configuration violation?
Allow user to do his own selections?

If you want to create custom diagnostics that will not pause for power configuration checks, answer N to the first query and possibly the second as well.

The third query affects the manner in which hardware modules are chosen for testing. The default, Y, lets the user select the modules to be tested, as in the normal case. If you specify N, you are not given the opportunity to select modules; instead, only hardware modules of a type already selected are tested.

MODULE SELECTION IN SP

The SP display is similar to that of the standard diagnostics. However, SP shows all the various types of hardware modules available for the system, not just those present at the time they are displayed.

There will be more modules in the SP display than will fit across the bottom of the screen, as indicated by three dots (...) at the right edge. The display scrolls when the cursor is moved off the right edge, revealing more modules. When the cursor is moved off the left edge, the display scrolls back.

SP allows dialogue queries to be marked and answered for modules that are not present, exactly as modules are tested in the standard diagnostics.

CHANGING DEFAULTS IN THE DIALOGUE

After you have marked the modules and pressed GO, SP proceeds with the initial dialogue for each marked module.

Instead of running tests, however, SP merely records the responses to the queries in an output file. When all the queries have been answered, SP writes the output file and then exits the program.

After running SP, the output file can be bootstrapped in the same way as the standard diagnostics. The responses given during the SP session become the default values. For example:

Enter the number of times to run the diagnostic: [l]

The normal default of [1] in this example could have been changed to some other higher number using SP.

SUPPRESSING QUERIES WITH SP

SP provides the ability to eliminate user intervention for one or all of the diagnostic queries. This feature is invoked by pressing CODE-S as the response to any of the questions instead of RETURN. The result is the suppression of any query during the execution of the custom diagnostics. For example:

Enter the number of times to ran the diagnostic: [10]

If you press CODE-S, the diagnostic runs ten times without asking you for permission.

Properly used, this feature makes it possible to set up custom diagnostics that run entirely unattended. This is particularly useful in systems that do not have a keyboard.

CAUTION

Since any query can be suppressed with CODE-S, potentially dangerous custom diagnostics can be created. If used unknowingly, they could destroy important disk data. Be careful with the distribution of these custom diagnostics so that data accidents do not occur.

SUPPRESSING QUERIES DURING THE ACTUAL DIAGNOSTICS

CODE-S can be used at any time, including during the standard diagnostics. Used in this way, CODE-S means "do not ask me this prompt again." However, reboot strapping the diagnostics restores the original default values, unaffected by CODE-S.

GLOSSARY

attribute state. The attribute state is a characteristic of the icon menu during various stages of the diagnostics. The six attribute states (displayed in the legend) are: untested, to be tested, testing, cursored, successful, and failed. See also legend.

bad spot. Bad spot refers to any part of a hard disk drive that is faulty.

bad spot data. Bad spot data is information included with a hard disk that is entered into the diagnostics to prevent an unnecessary failure of the tests. The diagnostics skips over the known bad spots when they are encountered, allowing a diagnostic test to fail only on a previously undiscovered flaw.

bit map. A bit map is a memory location storing a graphics image inside the Graphics Controller Module.

bootstrap. To bootstrap is to load the diagnostics into your workstation through a power-up or reset of your system. The diagnostics can be bootstrapped from a floppy disk drive or from a workstation where it has been previously installed. See also reset.

cluster. A cluster is a local resource-sharing network consisting of a master workstation and one or more distributed workstations.

CODEC. The CODEC is hardware that controls the conversion of analog-to-digital, and digital-to-analog signals inside the Telephone Manager Module.

color mapper. The color mapper is hardware inside the Graphics Controller Module that selects the colors available for display during the diagnostics.

configuration. The configuration is the arrangement of the modules, submodules, and hardware that make up your workstation. The configuration determines which tests can be run with the diagnostics and which icons appear on the screen. See also icons.

configuration rule. A configuration rule is a guideline for the proper operation of your workstation. If a configuration rule is violated and not corrected, your workstation may malfunction.

cylinder. A cylinder is a set of tracks on a storage device that can be accessed together as a unit.

default. A default is a value that is assumed by the diagnostics when no other value is given. A default remains in effect until it is changed or until the diagnostics is rebootstrapped.

diagnostics. The diagnostics is a collection of tests designed to detect improper operations or malfunctions of your workstation.

dialogue. The dialogue is the sequence of questions and answers initiated by the diagnostics before, during, and after the tests are run. The dialogue consists of queries and prompts. See also query and prompt.

DMA (direct memory access). DMA is hardware that allows a peripheral device to transfer data to or from memory without using the CPU.

DTMF generator/receiver. A DTMF generator/receiver is hardware that generates and receives Dual Tone Multi-Frequency signals inside the Telephone Manager Module. See also **Dual Tone Multi-Frequency signal**.

Dual Tone Multi-Frequency (DTMF) signal. A Dual Tone Multi-Frequency signal is a generated signal composed of more than one tone. It is used during certain diagnostic tests. See also **DTMF generator/receiver**.

error. An error is any mistake registered by the diagnostics. There are two kinds of errors. Soft errors occur intermittently; hard errors occur every time a test is run.

error code. See status code.

error message. An error message is a message containing information about specific errors during the diagnostics. It contains the applicable status codes, the controller status, and the number of hard and soft errors.

icon. An icon is a pictorial representation of a module or submodule in your workstation configuration. See also configuration.

icon menu. The icon menu is a pictorial representation of all the modules and submodules in your workstation configuration. You use the icon menu to select the tests and display the attribute states of the diagnostics. See also **icon** and **attribute state**.

initialize. Initialize means to place a module or device in its initial (start-up) state.

legend. A legend is a chart describing the attribute states, cursor movement keys, and type of Processor Module used in the diagnostics. The legend is located in the top window of the screen.

loopback connector. A loopback connector is an interface plug wired to specific pins so that an external port can be looped back to itself, completing a circuit. A loopback connector is necessary in order to run certain diagnostic tests.

loopback cord. A loopback cord is similar to a loopback plug and is used to complete an external circuit during certain diagnostic tests. However, the loopback cord uses more than one connector to complete the loop back to itself.

Memory Expansion Cartridge. A Memory Expansion Cartridge contains a RAM Memory Expansion Board. Up to three Memory Expansion Cartridges can be added to a Processor Module to provide up to 1M byte of RAM.

menu. A menu provides a choice of commands or operations that are available at a given time.

mode. A mode is the state of an application system or device set up to perform a specialized function. Each mode generally excludes the characteristics of any other mode.

Modular duplex jack. A modular duplex jack is a standard telephone connector with two input jacks, also known as an answering machine connector. It is used to attach two modular line cords to one telephone outlet. See also **modular line cord** .

modular line cord. A modular line cord is a standard telephone house cord with a standard telephone connector at both ends. It is available from the telephone company or most electrical supply stores.

module. A module is any one of several separate, identifiable units that connect your workstation and make up its configuration. See also **configuration** and **X-Bus**.

parallel (printer) I/O. A parallel (printer) I/O is an 8-bit parallel port used for I/O communications between your workstation and high speed devices, such as high speed printers.

parameter. A parameter provides the boundaries for an operation and allows you to enter or change information within those boundaries.

prompt. A prompt is a message from the diagnostics that tells you what actions to take before, or while running, the diagnostic tests. See also **dialogue**.

query. A query is any question asked by the diagnostics. See also **dialogue**.

register. A register is a temporary memory location for data.

Release Notice. The Release Notice is a document that accompanies the diagnostics disk and gives specific additional information about your version of the current software.

reset. Reset returns you to the original default values of the diagnostics. You can reset manually by holding down the spacebar and pressing the reset button on the back of the Processor Module. Alternatively, you can turn off the power and rebootstrap the system. See also **bootstrap**.

RS-232-C. RS-232-C refers to an industry specification developed to standardize the interface between different types of communications equipment.

RS-422. RS-422 is a high speed communications standard used to link cluster workstations.

scratch disk. A scratch disk is any blank or unneeded disk that can be erased or written to by the diagnostics. A scratch disk is placed in a floppy disk drive during the floppy disk drive tests.

sector. A sector is the smallest addressable portion of a track or band on a hard or floppy disk.

status code. A status code is a code number that reports the success or failure of a diagnostics operation. It appears on the screen as a two-, three-, or four-digit number and acts as a key to the type of error or malfunction that is encountered.

submodule. A submodule is a defineable component within a module that can be identified and tested independently of other components. An example is an RS-232-C port, which can be tested independently of other ports or submodules inside the Processor Module. See also **module** and **RS-232-C**.

window. A window is a distinct portion of the screen that is used to display a particular item or carry out a specific task. The diagnostics screen contains three windows.

X-Bus. The X-Bus is a standard, asynchronous system bus that allows configurability and interconnection between workstation modules. The X-Bus structure supports independent address spaces and allows modules of different speeds to interact. See also **module** and **configuration**.

INDEX

Page numbers in boldface indicate the principal discussion of a topic.

36-Volt Power Supply brick, 2-5

Attribute states, 2-4, 2-7

Bad spot data, 2-3, 5-11, 5-14 to 5-15
Barber pole tests, 3-9
Base memory test, 3-11
BFI, 5-14
Bootstrapping
  from a cluster, 2-2
  diagnostics, **2-2 to 2-3**
  Diagnostics Selection Program (SP), **A-1 to A-4**
  error, 2-4
  from a floppy disk, 2-3
  during keyboard tests, 9-2
  from a master, 2-3
  menu, 2-3
  to restore original values, 2-8
  standalone workstation, 2-3

CODEC test, **8-5**
Code-S, A-3
Color Monitor tests, **6-2 to 6-4**
Configuration
  rule, 2-2, 2-5
  violation, 2-2, 2-5
Cursored string test, 3-12
Cursor movement keys, 2-6

Damaging RS-422 cluster lines, 3-8
Debugger, 5-3, 5-14
Default values, 2-8
Destructive disk tests, 5-1, 5-11, A-4
  floppy disk, 5-5, 5-8
  hard disk, 5-16, 5-17,5-19
Diagnostics, introduction, 1-1
  manual organization, 1-1
  preconfiguration (SP), 1-1
  self-checking tests, 1-1
Diagnostics Selection Program (SP)
bootstrapping. A-1, A-3, A-4
  changing default values, A-1, A-4
  Code-S, A-3 to A-4
  danger of using, A-4
  custom diagnostics, A-1, A-2, A-3
  screen scrolling, A-2
  suppressing queries, A-1, A-3, A-4
Dialogue, initial, 2-8
Disk Expansion Module, 5-21
Disk Upgrade Module, 5-21
Dual Floppy Disk Module, **5-1 to 5-10**
  error message format, 5-9 to 5-10
  run full verification test, 5-2 to 5-3
  run quick verification test, 5-1
  selecting individual tests, 5-4 to 5-9;
  see also Individual disk tests
  disk functions, 5-6 to 5-8;
  see also Functions

Ending the diagnostics tests, 2-6, 2-10
Entering vendor code, importance of, 5-12
Errors
  hard, 2-4, 2-9, 5-10, 5-21, 8-1, 9-2
  messages, 2-2
  soft 2-4, 2-9, 5-20, 8-1, 9-2

Floppy disk controller, 5-9
Floppy/Hard Disk Module, **5-10 to 5-21**
  floppy disk tests, 5-10
  functions; **See** Functions
  hard disk tests, 5-11 to 5-21
  bad spot data, 5-14 to 5-15
  drive vendor code, 5-11
  run full verification test, 5-12
  run quick verification test, 5-12
  selecting individual tests, 5-15 to 5-20; **see also** Individual disk tests
  disk functions, 5-17 to 5-18; **see also** Functions
Font display test, 3-12
Functions
  floppy disk
  compare drive to drive, 5-8
  copy drive to drive, 5-7
  display/modify sector, 5-6
  loop on full track read, 5-8
  loop on sector read, 5-8
  loop on sector write, 5-8
  loop on track format, 5-8
  read disk address, 5-7
  read sequential tracks, 5-8
  read track format, 5-6
  hard disk
  display modify sector, 5-18
  loop on full track read, 5-18
  loop on sector read, 5-17
  loop on sector write, 5-17
  loop on track format, 5-17
  read boot ROM, 5-19
  read sequential tracks, 5-17 to 5-18

Graphics Controller Module, **7-1 to 7-13**
  attribute address test, 7-12 to 7-13
  graphics control register 1 and 2 tests, 7-2
  labels, 7-2
  line drawing test 1, 7-5 to 7-6
  line drawing test 2, 7-9
  lower and upper color mapper tests, 7-2
  memory test, 7-3
  overlapping lines test, 7-7
  pattern and vector mode test, 7-9 to 7-12
  clear mode, 7-12
  complement mode, 7-12
  replace mode, 7-12
  set mode, 7-9

Graphics Controller Module (**cont.**)
  stopping and starting the screen, 7-1 to 7-2
  three color test, 7-5
  with Color Monitor, 7-1
  with Monochrome Monitor, 6-1, 7-1

Hard disk controller, 5-20
Hard disk functions; **see** Functions
Hardware configuration, 2-4

Icon menu, 2-2, 2-3, 2-4, 3-13
Individual disk tests
  floppy disk
    format with verify, 5-5
    functions, 5-6 to 5-9
    random seek test, 5-4
    random write/read single sectors, 5-5
    recalibrate test, 5-4
    sequential seek test, 5-4
    sequential write/read multiple sectors, 5-5
    sequential write/read single sectors, 5-5
  hard disk
    format disk test, 5-16
    functions, 5-18 to 5-20
    random seek test with ID scan, 5-16
    random write/read single sectors, 5-17
    recalibrate test, 5-15
    sequential seek test, 5-16
    sequential write/read multiple sectors, 5-17
    sequential write/read single sectors, 5-17
    write/read all tracks, 5-16
Initial dialogue, 2-8

Keyboard tests, **9? to 9-4**
  echo test, 9-1
  I-Bus hardware reset, 9-2
    ID sequence, 9-2
    KBD software reset, 9-3
    loopback test, 9-3
     I-Bus position 02, 9-3 to 9-4
    ROM checksum, 9-3
  icon, 9-1
  LEDs, 9-1
  microcontroller, 9-3
  rebootstrapping the diagnostics during, 9-2

Legend, diagnostics, 2-7
Loopback connector, 3-3; **see also** RS-232-C

Mapped defects; **see** Bad spot data
Marking modules for test, 2-6
Media defects, 2-3; **see also** Bad spot data
Memory Expansion
  Cartridges tests, 3-1 to 3-2
Modules
  Disk Expansion Module, 5-21
  Disk Upgrade Module, 5-21

Modules (**cont**.)
Dual/Floppy Disk; **see** Dual Floppy Disk Module
Floppy/Hard Disk; **see** Floppy/Hard Disk Module
Graphics Controller; **see** Graphics Controller Module
Hard disk upgrades and expansions, 5-21
Multiline Port Expander, 3-3, 4-1
Processor; **see** Processor Module
selecting for test, 2-6
Telephone Manager; **see** Telephone Manager Module
Monitor tests, **6-1 -to 6-4**
Color Monitor, 6-2
color bar test 1, 6-3
color bar test 2, 6-3
speaker test, 6-4
stopping and starting the screen, 6-2
tests not self-checking, 6-2
Monochrome Monitor, 6-1
tests for Graphics Controller Module, 6-1
Monochrome Monitor tests, 6-1
Mosquito net test, 3-12
Multiline Port Expander Module, 3-3, 4-1

Offset, 5-14

Parallel (printer) I/O tests
printer error messages, 3-10
barber pole tests, 3-9
Power check configuration, 2-5
Power configuration, 2-5
Preliminary dialogue, 2-9
Printer
error messages, 3-10
maximum wait time, 3-9
Processor Modules, **3-1 to 3-13**
base memory test, 3-11
CPU timer test, 3-11
maximum printer wait time, 3-9
Memory Expansion Cartridge tests, 3-1 to 3-2
parallel (printer) I/O tests, 3-9 to 3-10
RS-232-C tests, 3-3 to 3-7; **see also** RS-232-C
RS-422 tests, 3-7 to 3-9; **see also** RS-422
Video controller tests, 3-11 to 3-13
same as for Monochrome Monitor, 3-11

Register
extended communications status, 3-7
floppy disk status, 5-9
hard disk error, 5-20
hard disk status, 5-20
RS-232-C control, 3-4
Release Notice, 2-2, 2-3, 5-11, 5-15, A-1
Reset button, 2-3
RS-232-C
asynchronous mode subtest, 3-4 to 3-5
bit/sync abort/idle subtest, 3-6
bit sync data transfer subtest, 3-5
character sync CRC-16 test, 3-5

RS-232-C (**cont.**)
control lines, 3-4
error information screen, 3-6
interface chip, 3-3, 3-4, 3-5, 3-6, 3-7
loopback plug, 3-3
ports, 3-3, 4-1
static status test, 3-4
RS-422
cluster maintenance mode subtest, 3-8 to 3-9
interprocessor data transfer subtest, 3-8
with active cluster, 3-8

Scratch disks, 2-1, 5-1, 5-11
Screen
scrolling, 2-4, 3-11
window formats, 2-4
Selection Program (SP); **see** Diagnostics Selection Program (SP)
Speaker test, 6-4
Stopping and starting the tests, 2-4, 3-11
Submodules, selecting for tests, 2-7

Telephone Manager Module, **8-1 to 8-8**
ADPCM encoder/decoder (CODEC) test, 8-5
analog crosspoint switch, 8-4, 8-5
call progress tone detector test, 8-5
DTMF generator/receiver, 8-2, 8-4
External Loopback test, 8-2 to 8-3
external telephone lines, 8-2, 8-6
icon menu, 8-1
internal loopback test, 8-3 to 8-4
inter-TM modem test, 8-1, 8-6 to 8-7
loopback cord, 8-2, 8-3
modular duplex jack, 8-2
modular line cord, 8-2
off-hook and on-hook relays, 8-2
standalone modem test, 8-5 to 8-6
Telephone Manager cord, 8-2
X-Bus DMA, 8-5, 8-7, 8-8
test, 8-8
Tests requiring visual verification, 1-1
Timer, CPU, 3-11
Troubleshooting, 1-1, 3-1, 5-1, 8-1, 9-1

Vendor code, 2-2, 5-11, 5-12, 5-21
Video controller cursored string test, 3-12
font display test, 3-12
mosquito net test, 3-12
same tests as for Monochrome Monitor, 3-11
video attribute test, 3-12
video memory test, 3-12
Video display appearance, 2-9
Visual verification, 1-1, 6-1, 6-2,7-1

Windows, 2-4

X-Bus
DMA; **see** Telephone Manager Module
overall length, 2-5

TABLE OF CONTENTS

Chapter	Title	Page
2	CRASH ANALYSIS	2-1
4	CTOS INITIALIZATION STATUS ANALYSIS	4-1
5	NGEN WORKSTATION BOOTSTRAP STATUS CODE	5-1
6	SRP BOOTSTRAP STATUS CODES	6-1
7	AWS-210 WORKSTATION BOOTSTRAP STATUS CODES	7-1
8	AWS-220/-230 WORKSTATION BOOTSTRAP STATUS CODES	8-1
9	AWS-240/COLOR WORKSTATION BOOTSTRAP STATUS CODES	9-1
10	IWS WORKSTATION BOOTSTRAP STATUS CODES	10-1
App. A	ACRONYMS	A-1

2 CRASH ANALYSIS

CRASH STATUS DESCRIPTION AND ANALYSIS

WORKSTATION CTOS CRASH STATUS DESCRIPTION AND ANALYSIS

When the CTOS operating system detects a fatal error condition, it reports the error. The boot ROM dumps memory to a crash file (if CrashDump.Sys exists) and the machine rebootstraps itself.

If the Debugger is configured into the operating system and is loaded in memory when the fatal error occurs, the operating system enters the Debugger before it performs a memory dump and rebootstrap. You can use the Debugger to investigate the cause of the fatal error. (See the Debugger Manual for more information.) You can also use the PLog command to review the error history of a workstation. (See the Executive Manual.)

When the operating system detects an error condition, your screen displays an error message. (If CTOS invokes the Debugger, the Debugger displays the error message again.) SysInit and Signon redisplay the crash information after system reboot. The information is also placed in the system log file, [Sys] <sys>Log.Sys. (Use the PLog command to display the log file.)

Each error message contains an error code in decimal and eight status words in hexadecimal. They are displayed in the following format:

```
CRASH STATUS (ERC xx.)  xxxx    xxxx   xxxx   xxxx
                        xxxx   xxxx   xxxx   xxxx
```

For example, if a fatal error 22 occurs while entering the debugger, the following error message can appear:

```
CRASH STATUS (ERC 22.)  006    0007   0000   0000   0004
                        000E    O34E   024F
```

The first status word contains the error code in hexadecimal form. The second word is the process number of the process that was running when the fatal condition occurred. The seventh and the eighth words contain the code segment (CS) and instruction pointer (IP) of the instruction following the procedure call to the CTOS fatal error handler, unless specified otherwise. The other four words are either unused, or have information unique to each error condition. (Status codes 22 through 27 in "Kernel," below, use these four words.)

SRP CTOS CRASH DISPLAY INTERPRETATION (REAR PANEL LEDs)

When the CTOS operating system detects a fatal error condition on the SRP that results in a crash, it rebootstraps itself and dumps each of the processors' memory to the appropriate crash files (if they exist).

CTOS system crash codes are displayed on the processor board rear LEDs after the crash (until the system is rebooted).

When the CTOS crash procedure (resident in each CTOS kernel) is called by a processor, an infinite loop is entered. The processor stays in this loop until it is reset by the master processor. This loop displays the 6 bit error code.

The beginning of a crash display loop is indicated by four cycles of a single LED (off) walking through the remaining seven LEDs (which are all on). See Figure 2-1, a below. Four display cycles follow this, with each cycle presenting one nibble (four bits) of the error code. At the end of the fourth nibble the entire loop repeats. See Figure 2-1, b-e.

Each nibble display cycle is indicated by a light on the top LED of the processor. (The top LED is labelled the SE bit.) When the top LED light is on, the bottom nibble (the four lower bits 3, 2, and 0) is read.

The bottom four LEDs indicate the value of the nibble (LED ON indicates a , LED OFF a 0). The most significant bit of the nibble is LED 3 and the least significant is LED 0. If the bottom four LEDs are off, the nibble value is 0. The most significant nibble is the first one that is displayed; the least significant is the last one. At the end of each nibble all the LEDs blink off. This indicates that the next nibble is about to be displayed.

To record a crash error code, wait for the beginning of a crash display loop: a single LED is off and walking through all the other LEDs, which are on, as indicated in Figure 2-1, a. When the single LED stops walking, write down the value of the bottom four LEDs each time the top LED goes on. This occurs four times as shown in Figure 2-l, b-e. Observe a second loop to verify that the values recorded are correct. For example, if a processor displays D, 7,B,9, the error code is 0D7B9h (h indicates hexadecimal). The loop occurs continuously until you reboot the system.

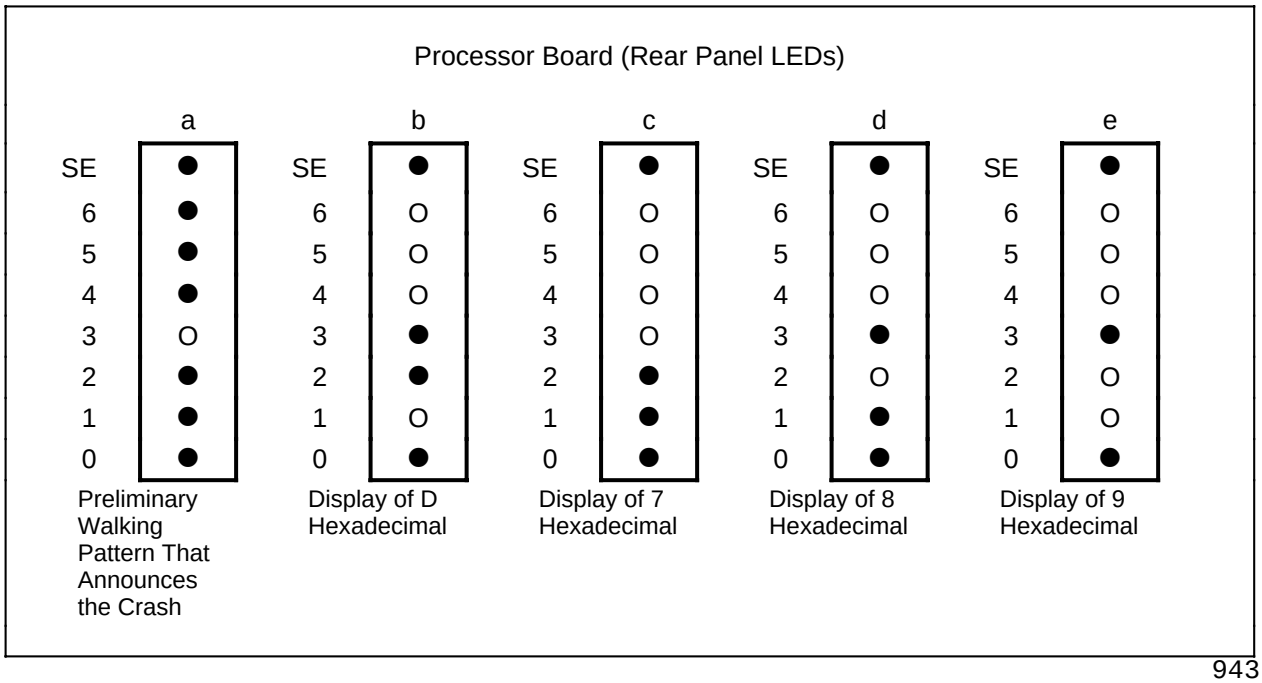


Figure 2-1. SRP Crash Display Loop.

SRP CTOS CRASH STATUS CODES INTERPRETATION

When an SRP CTOS crash occurs, the error log entry contains (8) hexadecimal words that further describe the error.

Word 1 Hexadecimal equivalent of the decimal ere.

Word 2 Process number of the process that was running when the error occurred. (This information may not apply when a hardware error occurs.)

Word 3 Contents of the Nonmaskable Interrupt (NMI) status register. This register is loaded when a nonmaskable interrupt occurs. The contents of this register can be decoded to determine specifics about the crash status that was reported. (The bits in the NMI status register are described below.)

Word 4 Contents of the memory location that was read when a double bit error occurred (ere 23).

Word 5 Contents of the Remote Slot register.

Word 6 Contents of base register 0. Base register 0 holds bits 6 to 3 of the off-board memory address. In the case or erc 23, this field contains the contents of the Error Correction Code (ECC) syndrome register.

Word 7 Contents of the CS register following the execution of the instruction that caused the crash.

Word 8 Contents of the IP register following the execution of the instruction that caused the crash.

Nonmaskable Interrupt Status Register

The contents of this register are reported above in Word 3 of the crash status codes.

Bit	Name		Meaning
15	ME	0 =	Memory expansion is installed.
14	SE	0 =	At least one board in the system is driving the system error line on the system bus.
13	LR	0 =	Last reset by power up or reset switch.
		=	Last reset by software.
12	NEM	0 =	If Nonmaskable Interrupt (NMI) was caused by a reference to a nonexistent memory location. The reference could have been initiated locally. It could have also been initiated by a processor or Direct Memory Access (DMA) controller on another board.
11	PF	0 =	Power fail.
10	TO	0 =	Bus timeout. No acknowledge was received from a memory or I/O timing circuit.
9	BE	0 =	Bus error. A remote double bit error or a nonexistent memory location.
8	DBE	0 =	Double bit memory error.
7	REM	0 =	The trapped address was generated by another board.
6	CAD	0 =	The trapped address was generated by the CPU.
5	DMA	0 =	The trapped address was generated by the local DMA controller.

Bit	Name		Meaning
4	DFP	1 =	This board is the designated File Processor.
3	REM	1 =	Panel switch is in remote. This is only applicable on the designated File Processor (EP) board.
2	NOR	1 =	Panel switch is in remote. This is only applicable on the designated EP board.
1	A9		Bit 9 of the trapped address.
0	A8		Bit 8 of the trapped address.

A9	A8	
0	0	Base Memory
0	1	Expansion Memory
1	1	Expansion Memory
1	1	Memory on another processor board

Sample Crash Status In System Log

ERC 22. Bus timeout. Cluster Processor (CP) in slot 74

	(1)	(2)	(3)	(4)	(5)
Status words:	0006h	0008h	DBA3h	0000h	0075h

(6)	(7)	(8)
000h	030h	0009h

(1) 6 hexadecimal = 22 decimal.

(2) Failure occurred in process whose hexadecimal value is 8 in this example.

(3) As indicated in the NMI status register display above:
Bit 0 Timeout.
Bit 6 CPU address.
Bit 1,0 Address greater than or equal to C0000h.

(4) Not used for this particular case.

(5) Board in slot 75 was being referenced.

(6) Memory lower than address EEEEh (64k) was being referenced.

(7) - (8) Instruction proceeding the instruction at address 0300:0009 was being executed when the timeout occurred.

4 CTOS INITIALIZATION STATUS ANALYSIS

The CTOS operating system tests the following hardware components during its initialization process:

- memory parity error detection circuitry
- memory
- keyboard
- interrupt circuitry
- programmable interval timer (PIT)

On IWS workstations the following hardware components are also tested during CTOS initialization:

- bus timeout circuitry
- video
- real time clock (RTC)

If the video test succeeds but any of the other tests fail, the following message appears on the screen:

```
INITIALIZATION ERROR STATUS wxyzh
```

Note that the following are three typical initialization errors:

80h	Keyboard is not plugged in
30h	Hardware memory failure
400h	Bad keyboard or typing during initialization

Each of the four digits in the error status word corresponds to a set of one or more error conditions detected during the test. Use the bit assignment chart below to determine which of the errors have occurred. Following the table are the meanings of the sixteen error conditions, numbered 0 through F (hexadecimal).

Bit assignment:

W	X	Y	Z
F E D C	B A 9 8	7 6 5 4	3 2 1 0

The operating system continues to load SignOn if any error other than a video error is detected. If the video test fails, the operating system halts and beeps 10 times. It also displays the error code in the LEDs on the keyboard (and on the I/O Memory board of IWS workstations).

IWS WORKSTATIONS

The LEDs on the I/O Memory board of IWS workstations are numbered according to the following convention: if you are standing in front of the workstation, and facing the LEDs on the I/O Memory board, the rightmost LED is LED 0 and the leftmost one is LED 5.

Error (bit)	**Meaning**
0 (LED F10)	IWS/NGEN: Video hardware does not respond. Possible causes are the following: 1. There is no video board. 2. The video board is not seated. 3. The cables are loose or not connected.
1 (LED F9)	IWS/NGEN: DMA failure in "load font."
2 (LED F8)	IWS/NGEN: DMA failure in "read font."

Error (bit)	**Meaning**
3 (LED F3)	IWS/NGEN: The font read back from the font RAM fails to compare with the font written to it.
4	Memory test failure.
5	Bus timeout interrupt is not generated when a nonexistent memory location is referenced.
6	Invalid memory parity is not detected.
7	Keyboard hardware does not respond. Possible causes are the following: 1. The keyboard is not connected. 2. The keyboard hardware is faulty.
8	Keyboard does not return good status after the reset command. Possible causes are the following: 1. Keys were pressed during the initialization. 2. The keyboard hardware is faulty.
9	Keyboard ROM checksum failure.
A	Keyboard loopback test failure.
B	Keyboard interrupt test failure. No interrupt is generated during loopback, or TRANSMIT READY status in 8251A does not generate interrupt.

Error (bit)	**Meaning**
C	Real-Time Clock (RTC) test failure. No interrupt, or time interval between two RTC interrupts in inconsistent with the time interval measured by PIT.
D	Programmable interval timer (PIT) test failure. No PIT interrupt.
E	Continuous PIT interrupts.
F	Communications hardware test failure (cluster or master workstation only).

5 NGEN WORKSTATION BOOTSTRAP STATUS CODE

INTRODUCTION

When the workstation is bootstrapped, it goes through diagnostic and bootstrapping routines, which are resident in the ROM of the CPU. When an error is detected by the bootstrap ROM, the error code appears on the screen. For E0h and E1h error codes only, the workstation beeps five times and the error code appears on the keyboard LEDs. (An E0h error code indicates a bad ROM, and an E1h error code indicates a bad RAM.)

ERRORS DURING BOOTSTRAP OR DUMP

The communications bootstrap or dump routines do not stop to report an error if there is no activity on the RS-422 cluster communications line. An error can occur when the cable to the master workstation is disconnected, when the master workstation fails, or when the master workstation is disabled by the Disable Cluster utility. When the connection with the master workstation is reestablished, the bootstrap or dump routine automatically starts (shown on the screen by a period (.) for every sector transferred).

INTERPRETING KEYBOARD CODES

The E0h and E1h error codes are displayed on the keyboard LEDs. OVERTYPE is the most significant and f10 is the least significant. Interpret them as follows:

LED	Error E0h	Error E1h
OVERTYPE	on	on
LOCK	on	on
fl	on	on
f2	off	off
f3	off	off
f8	off	off
f9	off	off
f10	off	on

CODE LISTING

The error codes are listed in hexadecimal format below. There is also a list of possible causes for most of the errors. (The causes are listed with the most likely one first.)

For more information see

Diagnostics Manual

Status Code (hexadecimal)	Meaning/Possible Causes
00 to 01	Reserved for future use.
02	No floppy controller. Processor cannot communicate with floppy controller. Check: The Dual Floppy Disk Module connection to X-Bus
03	Timeout waiting for an interrupt after a Seek command. The floppy disk controller did not interrupt the CPU after being issued a Seek command. Check: • that the user did not open the door of the floppy disk drive • that the user did not open the Dual Floppy Disk Module connection to X-Bus
04 to 05	Reserved for future use.

Status Code (hexadecima1)	Meaning/Possible Causes
06	DMA never finished. The Byte Count register of the 80186 DMA Channel 0 never decremented to 0, which means that the DMA operation never finished. Check: • the CPU board (Processor Module) • the Dual Floppy Disk Module (8253, WD2797)
07 to 08	Reserved for future use.
09	Run file checksum error. Floppy disk contains no run file. Check: • the CPU board (Processor Module) • the Dual Floppy Disk Module
0A	File header invalid. The System Image file on the floppy disk does not contain a valid run file. Since the Initialize Volume utility does not automatically copy a System Image file onto the volume it is initializing, the user must copy a valid System Image file onto the volume. Check: the floppy disk

Status Code (hexadecimal)	Meaning/Possible Causes
0B	Floppy Control register inconsistent. The Status register was polled until it became ready. The Floppy Status register was polled again, and it was not ready. Check: the dual floppy controller (WD2797)
0C	Floppy disk drive became not ready during a seek. The floppy disk drive became not ready while performing a Seek command. This error can be caused by opening the door of the floppy disk drive or by a bad cable from the floppy disk drive to the motherboard. Check: • user intervention • the cable from the floppy disk drive to the floppy disk controller • the floppy disk drive • the dual floppy controller (WD2797)
0D to 0E	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
0F	Floppy disk drive fault condition during a Seek or Recalibrate command. The floppy disk drive did not recalibrate to track 00 after 77 step pulses, or the drive fault line went active. Check: • the cable between the floppy disk drive and the Floppy Disk Controller board • the floppy disk drive • the dual floppy controller (WD2797)
10	Abnormal termination of Seek command. The floppy disk drive did not complete the Seek command correctly. Either the floppy disk drive failed, or the ready status changed. Check: • user intervention • the floppy disk • the cable between floppy disk drive and Floppy Disk Controller board • the floppy disk drive • the dual floppy controller (WD2797)

Status Code (hexadecimal)	Meaning/Possible Causes
11 to 12	Reserved for future use.
13	Floppy disk drive not ready. The floppy disk drive was not ready when a Read or Write command was issued. This error can only occur if the floppy disk drive was ready during a previous Recalibrate command and a previous Seek command. Check: that the disk was not removed
14	Reserved for future use.
15	End of track. After a Read or Write command, no Terminal Count signal was received from the DMA. Check: • the cable between the floppy disk drive and Floppy Disk Controller board • the CPU board (Processor Module) • the dual floppy controller (8253)
16	Data error (data field). The floppy disk drive controller cannot read data from the floppy disk drive correctly.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the floppy disk • the cable between floppy disk drive and Floppy Disk Controller board • the floppy disk drive • the dual floppy controller (WD2797)
17	Data error (identification field). The floppy disk drive controller cannot read the identification field of the addressed sector. Check: • the floppy disk • the cable between floppy disk drive and floppy disk controller • the floppy disk drive • the dual floppy controller (WD2797)
18	Data late. The floppy disk drive controller did not get service from the DMA in time.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the seating of the CPU on the motherboard • the CPU board (Processor Module) • the dual floppy controller (WD2797) • the Dual Floppy Disk Module connection to the X-Bus
19 to 1B	Reserved for future use.
1C	Floppy disk write protected. This error code appears only during the dump operation. It indicates that the floppy disk has a write protect tab in place. Check: the floppy disk
1D to 1E	Reserved for future use.
1F	Abnormal termination of command. The floppy disk drive controller reported abnormal termination of a command without reporting the cause. Check: the dual floppy controller (WD2797)

Status Code (hexadecimal)	Meaning/Possible Causes
20	Incompatible processor. A disk module is incompatible with the processor. Use a later revision disk module with this processor.
21 to 22	Reserved for future use.
23	Timeout waiting for an interrupt. The hard disk controller did not interrupt the CPU after being issued a command. Check: • the Floppy/Hard Disk Module connection to the X-Bus • the Hard Disk Controller board • the CPU board (Processor Module)
24 to 25	Reserved for future use.
26	DMA not done. The Word Count register of the 8237 DMA Channel 3 never decremented to 0FFFFh, which means that the DMA operation never finished. Check: • the CPU board (Processor Module) • the hard disk controller (8253s, WD1010)

Status Code (hexadecimal)	Meaning/Possible Causes
27	No valid Volume Home Block. No Volume Home Block could be found within the first track of the disk. Check: that the disk was initialized by the Initialize Volume utility
28	No file. No System Image or Crash Dump file exists. Check: that the disk was initialized by the Initialize Volume utility
29	Run file checksum error. The System Image file on the hard disk failed a checksum test. Check: • that a valid run file was copied to the System Image file • the Memory board and Memory Expansion Cartridges (Processor Module) • the CPU board (Processor Module) • the Floppy/Hard Disk Module

Status Code (hexadecimal)	Meaning/Possible Causes
2A	File header invalid. The System Image file on the hard disk does not contain a valid run file. Since the Initialize Volume utility does not automatically copy a System Image file onto the volume it is initializing, the user must copy a valid System Image file onto the volume. Check: the hard disk System Image file
2B	Hard disk Status register inconsistent. The status register was polled until it became ready. The Status register was then polled again and it was not ready. Check: the Hard Disk Controller board (WD1010)
2C	No Seek complete. The Seek complete status was not set after an implied seek. Check: • The cable from the hard disk drive to the hard disk controller motherboard • The hard disk driver • The hard disk controller (WD1010)

Status Code (hexadecimal)	Meaning/Possible Causes
2D to 30	Reserved for future use.
31	Drive not ready. The hard disk drive became not ready during an operation. Check: • the cable from the hard disk drive to the hard disk controller motherboard • the hard disk drive • the hard disk controller (WD1010)
32	Reserved for future use.
33	Hard disk controller not ready. The hard disk controller remained in a busy state after a write or read operation should have completed. Check: • the hard disk controller (WD1010) • the hard disk drive
34	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
35	Sector not found. The hard disk controller could not locate a particular sector on a track. Check: • that the hard disk drive has been formatted • the cables between the hard disk drive and hard disk controller • the hard disk controller (WD1010) • the hard disk drive
36	Data error (data field). The hard disk controller could not read data from the hard disk drive correctly. Check: • that the hard disk drive has been formatted • the cables between the hard disk drive and hard disk controller • the hard disk controller (WD1010) • the hard disk drive
37	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
38	Data late. The hard disk drive controller did not get service from the 8237 DMA controller in time. Check: • the seating of the CPU board on the Processor Module motherboard • the CPU board (Processor Module) • the hard disk controller (WD1010) • the Floppy/Hard Disk Module-connection to the X-Bus
39 to 3B	Reserved for future use.
3C	Hard disk write fault. This error code appears only during the dump operation. Check: • the cables from the hard disk drive to the motherboard • the hard disk controller (WD1010) • the hard disk drive
3D to 3E	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
3F	Abnormal termination of command. The hard disk drive controller reported abnormal termination of a command without reporting the cause. Check: The hard disk controller (WD1010)
40	Input/output error or bad tape cartridge. The tape cartridge is unreadable. Check: • the cartridge and, if necessary, try a new one • that the tape drive heads are clean and clean them if they are not
41	Unexpected interrupt from the tape controller. Check: the Tape Interface board
42	Bad run file signature. The run file on the cartridge is not valid. Recopy the run file to the tape with the Tape Copy command.

Status Code (hexadecimal)	Meaning/Possible Causes
43	Tape controller timeout. The tape controller is not responding. Check: the tape interface card and the tape drive
44	Not enough memory. The run file being booted from tape is larger than available memory. Add more RAM to the system.
45	Run file checksum error. The run file is bad. • Recopy the run file to the tape. • Try a new tape cartridge.
46 to A2	Reserved for future use.
A3	Serial input/output error. The serial input/output initialization routine detected an error in the serial input/output communications controller chip. Check: • the I/O board (Processor Module) • the CPU board (Processor Module)

Status Code (hexadecimal)	Meaning/Possible Causes
A4	8254 error. The clock initialization routine detected an error in the 8254 programmable counter/timer chip. Check: the CPU board (Processor Module)
A5	No SIM. RIM was sent to the master workstation, but no SIM was received. This indicates that the workstation is able to receive but not transmit, or that the master workstation is able to transmit but not receive. Check: • the cluster communications logic on the I/O Board (Processor Module) • the master workstation • the communications cable • the operating system of the master workstation, which may have crashed
A6	No UP in initialization (SNRM). A UA or XID was sent to acknowledge the SIM sent by the master workstation, but the master workstation sent back an SNRM instead of a UP. The master workstation probably timed out, while waiting for the UA or XID.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the I/O board (Processor Module) • the master workstation • the communications cable • the operating system of the master workstation, which may have crashed
A7	No UP in initialization (DISC). A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back a DISC instead of a UP. Check: • the I/O board (Processor Module) • the master workstation • the communications cable • the operating system of the master workstation, which may have crashed
A8	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
A9	No identification available. The initialization routine monitored the cluster communications line but did not find a free identification number. This is usually caused by attaching more workstations to a cluster communications line than the operating system of the master workstation is designed to accept. Check: the operating system of the master workstation, which may have crashed
AA	Identification failure. The initialization routine found free workstation identification numbers by monitoring the communications line. but errors were detected when it tried to use one. This is usually caused by a failure of the collision recovery algorithm and can be overcome by pressing the reset button on the back panels of each workstation involved in the collision.
AB	Read identification timeout. The initialization routine timed out after waiting 10 seconds while monitoring the communications line for a workstation identification number. This error code is generated only after a number of unsuccessful reads.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the I/O board (Processor Module) • the master workstation • the communications cable • the operating system of the master workstation, which may have crashed
AC	Bad address (dump routine). The workstation identification number sent in a frame by the master workstation did not match the one expected. Check: • the communications cable • the I/O board (Processor Module)
AD	Disconnected (dump routine). The master workstation sent a DISC because of excessive lines or protocol errors or because of a conflict with the crash/dump file at the master workstation.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • that either the file [Sys]<Sys> WSnnn>CrashDump.Sys or [Sys] <Sys>WS>CrashDump.Sys at the master workstation exists • that the file is not in use by another workstation that is dumping • that the file is large enough • the communication cable • the I/O board (Processor Module)
AE	No UP - SNRM. Check: • the I/O board (Processor Module) • the master workstation
AF	No UP - REJ. Check: • the I/O board (Processor Module) • the master workstation
B0	No UP. After transmitting a dump block, an unexpected response was received from the master workstation. Check: • whether a cluster work-station is using the fixed identification mode • the I/O board (Processor Module)

Status Code (hexadecimal)	Meaning/Possible Causes
B1	Read UI error. A bootstrap block (frame type UI) was expected, but another frame type was received. Check: the I/O board (Processor Module)
B2	Read SNRM error. A bootstrap block (frame type UI) was expected, but a SNRM was received. Check: the I/O board (Processor Module)
B2	Read SNRM error. A bootstrap block (frame type UI) was expected, but a SNRM was received. Check: the I/O board (Processor Module)
B3	Disconnected. The master workstation chose to send a DISC because of a conflict with the System Image file, or because of excessive errors during transmission. Trying to bootstrap a nonexistent operating system can cause this error to occur.

Status Code (hexadecimal)	Meaning/Possible Causes
	Operating system number 252 is used for a workstation with no mass storage. Number 251 is used for a workstation with floppy disk storage only. Number 250 is used for a workstation with both floppy and hard disk storage. Check: • that there is a [Sys]<Sys>WSnnn >SysImage.Sys file at the master workstation for the workstation type selected (nnn). The master workstation does not have the operating system requested. If /[Sys]<Sys]WSnnn>SysImage.Sys cannot be found, the default System Image file [Sys] <Sys>WS> SysImage.Sys is loaded. • the cluster communications cables • the I/O board (Processor Module)
B4	Bad checksum of System Image file. The System Image file transferred from the master workstation is not a valid run file. Either the file is invalid, or the transmission was faulty or incomplete.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • whether the operating system of the cluster workstation is invalid • the I/O board (Processor Module) • the CPU board (Processor Module) • the Memory board (Processor Module)
B5	Read error. Excessive input/output errors occurred while the bootstrap interface block was being read. Check: • the I/O board (Processor Module) • the cluster communications cables
B6	Read timeout. During a read operation, no response was received from the master workstation. Check: the operating system of the master workstation, which may have failed
B7	Write DMA count is bad. After completion of a write operation, the bootstrap ROM determined that the entire block was not sent.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the I/O board (Processor Module) • the CPU board (Processor Module)
B8	Write timeout. A write operation did not properly complete. Check: the I/O board (Processor Module)
B9	Bad bootstrap block format. A bootstrap block of an invalid length was received. Check: whether the format of the bootstrap file is correct
BA	DMA error. After initializing the DMA channel for a Read or Write operation, the DMA controller did not contain the same information that was written to it. Check: the CPU board (Processor Module)

Status Code (hexadecimal)	Meaning/Possible Causes
BB to DF	Reserved for future use.
E0	ROM checksum error. There is a bad 2732 ROM on the CPU board. This error is displayed on the keyboard LEDs, not the video display. (See "Interpreting Keyboard Error Codes," above.) Check: the CPU board (Processor Module)
E1	RAM error. There is a failure in the bootstrap ROM's RAM work area. The bootstrap ROM uses this work area to compose error codes. If a failure occurs, this error appears on the keyboard LEDs, not on the screen. (See "Interpreting Keyboard Error Codes," above.) Check: the CPU board (Processor Module)
E2	RAM read and write 0's error. See E4 below.
E3	RAM read and write 1's error. See E4 below.

Status Code (hexadecimal)	Meaning/Possible Causes
E4	RAM read and write address error. This explanation applies to codes E2, E3, and E4. An error occurred during the read and write RAM test. All 1's, all 0's, or an address pattern are written, read, and compared. The comparison showed that the data written and read were not identical. Note that if a failure is confined to a small number of memory locations, the likely source of the failure can be derived from the high-order bit of the failed addresses. The high-order addresses in the Processor Module are: 0-3 Memory board 4-7 1st RAM Expansion Cartridge 8-B 2nd RAM Expansion Cartridge C-F7 3rd RAM Expansion Cartridge F8-F9 Video RAM FA-FB Font RAM The error display for E2, E3, E4, and E5 (below) is: E: E2 1000:675C 0000 0002

Status Code (hexadecimal)	Meaning/Possible Causes
	E: E2 = the error code 1000:675C = the hexadecimal address 0000 = the expected value 0002 = the received value Check: • the Memory board (Processor Module, includes expansion) • the CPU board (Processor Module) • the motherboard for any module connected on the X-Bus
E5	RAM address test error. An error occurred during the RAM addressing test. After completion of the RAM read/write address test, each RAM word should contain the sum of its own address. The RAM address test verifies that this is still true after one complete cycle of the test. This error can be caused by a short or a shorted address line allowing different RAM locations to respond to the same CPU. It may also be caused by memory that picks up or drops bits when idle. Check: • the Memory board (Processor Module) • the RAM Expansion Cartridges (Processor Module)

Status Code (hexadecimal)	Meaning/Possible Causes
E6	Keyboard initialization error. An error occurred while the bootstrap ROM was initializing the hardware. Check: • the Video board (Processor Module) • the I/O board (Processor Module)
E7 to FF	Reserved for future use.

6 SRP BOOTSTRAP STATUS CODES

INTRODUCTION

When the system is bootstrapped it goes through diagnostic and bootstrapping routines that are resident in the ROM of the master processor (MP). (The MP can be either a Data Processor or a File Processor.)

FRONT PANEL NUMERIC DISPLAY

In the course of normal booting, the lights cycle from 00 to 20 in the two-digit front panel display. This panel display is in the primary enclosure of the SRP system. Any values beyond 20 indicate an error condition.

The front panel codes indicate the following:

- Codes 00 to 05 show progress status codes. You see these codes during any normal boot sequence while the bootstrap ROM is executing.
- Codes 06 to 20 indicate that the bootstrap ROM has completed its job and the operating system has taken over to initiate the remainder of the software initialization procedure.
- Codes 21 to 29 indicate that no valid boot media is currently on the system and that the user must insert a valid cartridge (either disk or tape, whichever is appropriate).
- Codes 30 to 39 indicate a hardware error detected by the boot ROM. This prevents a successful boot
- Codes 40 to 50 indicate a software operating system crash. (Look at the rear panel "walking code" and see Section 2, "Crash Analysis.")

CODE LISTING FOR FRONT PANEL STATUS CODES

For more information see

Megaframe CTOS Administrator's Manual

Megaframe CTOS Programmer's Guide

Mega frame Hardware Manual

> NOTE
>
> Status codes 01 to 20 are displayed on the front panel LEDs during the boot ROM self-test and initialization sequence. These codes do not indicate errors.

Status Code (hexadecimal)	Meaning/Possible Causes
00	System is in the reset mode (key is in the STOP position).
01	Boot ROM is performing initial hardware checks. These checks include the "Error Correction Code wash" ("ECC wash"). (The rear LEDs provide details about this progress. See Rear LED Codes below.)
02	Boot ROM is writing the optional [Sys]<sys>crashDump.sys file.
03	Boot ROM is performing a full memory read/write test.

Status Code (hexadecimal)	Meaning/Possible Causes
04	ROM is now booting the master processor system image file. [sys]<sys>SysImage.sys. into memory and relocating it.
	While the ROM is waiting for a disk (or cartridge) to become ready, the display alternates between A1 and 04.
05	Boot ROM sequence has completed successfully.
	The System Image file will now be initiated.
06	Operating system initialization has begun.
07	Hardware initialization is complete.
08	Kernel initialization is complete.
09	Process initialization is complete; interrupts are about to be enabled.
10	Processor downloads are in process.
	All initialization is complete.
20	System is running and functioning normally.

Status Code (hexadecimal)	Meaning/Possible Causes
21	ROM is unable to boot from any of the fixed disks and a cartridge has not been inserted.
23	ROM did not find any Volume Home Block (VHB) on the first ready drive.
24	ROM found a bad run file signature on the first ready drive.
25	Bad run file checksum (of the system image) on the first ready drive.

NOTE

Errors 26 to 29 appear only when a Data Processor (DP) is the master Processor, such as in an SRP E Enclosure. These errors also appear on the rear panel.

26	Error when trying to reset.
27	Error when trying to rewind tape.
28	Error when reading tape.
29	Tape was written with incorrect/ unsupported blocking factor.
30	Disk error on drive 0.

Status Code (hexadecimal)	Meaning/Possible Causes
31	Disk error on drive 1.
32	Disk error on drive 2.
33	Disk error on drive 3.
36	Bad disk controller. ROM could not read the controller registers.
37	Bad disk controller. The controller was never ready in the command phase of the disk operation.
38	Bad disk controller. The controller did not respond after a command was issued.
39	General hardware error. See rear LEDs for the specific error.
40	CTOS detected a fatal error on a File Processor (FP) board. This error could either be a reported failure to complete initialization or a failure detected by the watchdog function after initialization had completed.

Status Code (hexadecimal)	Meaning/Possible Causes
41	CTOS detected a fatal error on a Terminal Processor (TP) board. (See error 40 above.)
42	CTOS detected a fatal error on a Cluster Processor (CP) board. (See error 40 above.)
43	CTOS detected a fatal error on a Storage Processor (SP) board. (See error 40 above.)
44	CTOS detected a fatal error on an Application Processor (AP) board. (See error 40 above.)
45	CTOS detected a fatal error on a processor of an undetermined type. This may occur during the process of booting the other boards in the system. If one board is malfunctioning and making it difficult to determine the processor type, then this is the front panel state. You should consult the back panel LEDs of all the processors to see which board is not responding properly during the boot sequence.
50	Fatal software error has occurred. The low 8 bits of the error code (erc) is found in the rear LEDs.

Status Code (hexadecimal)	Meaning/Possible Causes
E0	This value alternates with the enclosure number (the first B box is enclosure 2) to indicate that power for that enclosure has not yet been applied.
DE	The system is in degraded mode. Initialization failed on one or more boards, or the power could not could go on for one or more enclosures.

REAR PANEL LED CODES

When an error is detected by the bootstrap ROM, the error code appears on the rear panel LEDs.

NOTE

The rear LEDs display software crash codes, as well as boot ROM codes. The rear LEDs also display each of four hexadecimal digits which make up the error code. To determine if the code is a software crash code or a boot ROM error code, watch the lights as the system initializes. If the LEDs "walk" or rotate, then it is a software crash code. If the LEDs are constant, it is a boot ROM code. On the master processor (MP), errors that occur before the front panel lights read 07 are boot ROM errors.

The LED pattern should remain static only during bootstrap time. If you see the lights "freeze" after the system has been running for ten minutes or more, the system or hardware is malfunctioning.

The codes displayed in the rear LEDs are described below. The LEDs are interpreted as one hexadecimal byte. The most significant bit is the topmost LED on the board. The corresponding front panel is given which applies when these rear LED codes appear on the MP. (During the bootstrap ROM process the LEDs display a fixed pattern.)

Codes 01 to 07 and 10 below, do not indicate an error condition. They can be used as an aid in diagnosing problems. The lights should cycle through these numbers but not stop at them. An error condition occurs when the numbers are fixed in any of these values, for any length of time.

Codes from 01 to 07 will have 01 displayed on the front panel.

Status Code (hexadecimal)	**Meaning/Possible Causes**
01	Starting hardware initializations; performing ROM checksum.
02	Performing initial memory check of first 64k of RAM.
03	Setting up initial memory area.
04	Determining memory size.
05	Relocating CTOS save buffer; setting up Computer Definition Table.
06	Checking I/O ports.
07	Performing ECC "wash" to set check bits correctly.
10	Hardware testing completed.

Status Code (hexadecimal)	Meaning/Possible Causes
Errors from 0A to 0F will have 39 displayed on the front panel.	
0A	Bad ROM checksum.
0B	Bad I/O ports. The boot code could not successfully write and read back port 40 (Remote Slot), port 48 (BRO), and port 50 (BR1).
0C	Memory error in on-board memory while writing zeros.
0D	Memory error in on-board memory while writing ones.
0E	Memory error in on-board memory while writing addresses.
0F	Memory error in on-board memory while verifying addresses.
Errors from 21 to 23 will have 21 displayed on the front panel.	
21	Valid bootable cartridge must be inserted.
22	No tape or disk devices contain a valid boot image.
23	No valid VHB found (on the first ready drive).

Status Code (hexadecimal)	Meaning/Possible Causes
Errors from 24 to 25 will have 21 displayed on the front panel.	
24	Bad run file signature (on the first ready drive).
25	Bad run file checksum (on the first ready drive).

NOTE

Errors 26 to 29 appear only when a DP is the master processor, such as in an SRP E Enclosure. These errors will also appear on the front panel.

26	Error when trying to reset.
27	Error when trying to rewind tape.
28	Error when reading tape.
29	Tape was written with incorrect/ unsupported blocking factor.
30	Disk error on drive 0.
31	Disk error on drive 1.
32	Disk error on drive 2.
33	Disk error on drive 3.

Status Code (hexadecimal)	Meaning/Possible Causes
Errors from 36 to 38 will have 39 displayed on the front panel.	
36	Bad disk controller. The controller registers cannot be accessed correctly.
37	Bad disk controller. The controller was never ready in the command phase of the disk operation.
38	Bad disk controller. The controller did not respond after a command was issued.

NOTE

Errors 3A to 3B appear only when a DP is the master processor, such as in the SRP E Enclosure.

These errors will have a 39 on the front panel.

3A	Master Storage Processor (SP) does not have a Storage Controller (SC) attached.
3B	Inconsistent values on SMD Controller interface.

Status Code (hexadecimal)	Meaning/Possible Causes

NOTE

Errors 3C to 3D appear only when a DP is the master processor, such as in the SRP E Enclosure.

These errors will have a 39 on the front panel.

3C	SMD Controller Data Input / Output (DIO) bit set incorrectly.
3D	A fatal SMD I/O error has occurred. (This is a generic error.)

Errors from 4C to 4F will have 39 displayed on the front panel.

4C	Memory error in expansion memory while writing zeros.
4D	Memory error in expansion memory while writing ones.
4E	Memory error in expansion memory while writing addresses.
4F	Memory error in expansion memory while verifying addresses.

REAR PANEL LEDS FOR THE NONMASTER PROCESSORS

If the nonmaster boot ROMS successfully pass all bootstrap ROM internal tests, the processor boards wait to be reset and/or booted. (File Processor (FP) , Terminal Processor (TP), Cluster Processor (CP), and Storage Processor (SP) are examples of non-master processors.) When this occurs the boot ROM "walks" its LEDs from top to bottom. If a single LED is walking, no Memory Expansion board is connected. If two nonadjacent LEDs are walking, a Memory Expansion board is connected.

Although the preceding applies to all 186-based processor boards, there are some additional LED patterns implemented for the Storage Processor boot ROMs. If two adjacent LEDs are walking, then a Storage Controller (SC) is connected to the SP, but there is no memory expansion. If three adjacent LEDs are walking, then both an SC and Memory Expansion board are connected to the Storage Processor. This is summarized below:

LED walking pattern			**Meaning**
On	Off	Off	No other boards are connected.
On	Off	On	Memory Expansion is connected.
On	On	Off	Storage Processor has Storage Controller connected.
On	On	On	Storage Processor has Storage Controller and Memory Expansion board connected.

7 AWS-210 WORKSTATIN BOOTSTRAP STATUS CODES

INTRODUCTION

When the workstation is bootstrapped, it goes through diagnostic and bootstrapping routines that are resident in the ROM of the CPU. When an error is detected by the bootstrap ROM, the error code appears either on the video display or on the keyboard LEDs. For E0h and E1h error codes only, the workstation beeps on and off five times. (An E0h error code indicates a bad ROM, and an E1h error code indicates a bad RAM.)

NO ACTIVITY DURING BOOTSTRAP OR DUMP

The bootstrap or dump routines do not stop to report an error if there is no activity on the RS-422 cluster communications line. This can occur when the cable to the master workstation is disconnected, when the master workstation crashes, or when the master workstation is disabled by the Disable Cluster utility. When the connection with the master workstation is reestablished, the bootstrap or dump routine automatically starts (indicated on the video display by a period (.) for every sector transferred).

INTERPRETING KEYBOARD CODES

The error code displayed on the keyboard LEDs is interpreted as an 8-bit value with the following assignments:

LED	Bit
OVERTYPE (OT)	7 (most significant bit)
LOCK (LK)	6
fl	5
f2	4
f3	3
f8	2
f9	1
f10	0 (least significant bit)

CODE LISTING

The error codes are listed in hexadecimal format below. There is also a list of possible causes for most of the errors. (The causes are listed with the most likely one first.)

For more information see

AWS-210 Hardware Manual

Status Code (hexadecimal)	Meaning/Possible Causes
00 to A2	Reserved for future use.
A3	Serial input/output error. The serial input/output initialization routine detected an error in the serial input/output communications controller chip. Check: the CPU board (7201)
A4	8253 error. The clock initialization routine detected an error in the 8253 programmable counter/timer chip. Check: the CPU board (8253)
A5	No Set Initialization Mode (SIM). Request Initialization Mode (RIM) was sent to the master workstation, but no SIM was received. This indicates that the workstation is able to receive but not transmit, or the master workstation is able to transmit but not receive.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the Communications cable • the operating system of the master workstation (for a crash)
A6	No UP in initialization (SNRM). A UA or XID was sent to acknowledge the SIM sent by the master workstation, but the master workstation sent back an SNRM instead of a UA. The master workstation's time limit most likely expired waiting for the UA or XID. Check; • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A7	No UP in initialization (DISC). A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back a DISC instead of a UA.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A8	No UP in initialization. A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back something other than a UA. Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A9	No identification available. The initialization routine monitored the cluster communications line but never found a free identification number. This is usually caused by attaching more workstations to a cluster communications line than the operating system of the master workstation is designed to accept.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: whether the operating system of the master workstation has crashed
AA	Identification failure. The initialization routine found free identification numbers by monitoring the communications line, but errors were detected when it tried to use one. This is usually caused by a failure of the collision recovery algorithm and can be overcome by pressing the reset button on the rear panel of the workstations that collided.
AB	Read identification timeout. The initialization routine's response time limit expired after waiting 10 seconds while monitoring the communications line for an identification number. This error code is generated only after a number of successful reads. Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)

Status Code (hexadecimal)	Meaning/Possible Causes
AC	Bad address (dump routine). The workstation identification that was sent in a frame by the master workstation did not match the one expected. Check: • the communications cable • the CPU board
AD	Disconnected (dump routine). The master workstation sent a DISC because of excessive line or protocol errors, or because there was a conflict with the crash/dump file at the master workstation. Check: • whether the file [Sys]<Sys>WS> CrashDump.Sys at the master workstation (a) does not exist, (b) is in use by another workstation that is dumping, or (c) is not large enough • the communications cable • the CPU board
AE	No UP - SNRM. See B0 below for explanation.
AF	No UP - REJ. See B0 below for explanation.

Status Code (hexadecimal)	Meaning/Possible Causes
B0	No UP. This explanation applies to codes AE, AF, and B0. After transmitting a dump block, an unexpected response was received from the master workstation. Check: • whether an IWS cluster workstation is using the fixed identification mode • the CPU board (7201)
B1	Read UI error. A bootstrap block (frame type UI) was expected but another frame type was received.
B2	Read SNRM error. A bootstrap block (frame type UI) was expected but an SNRM was received. Check: the CPU board (7201)
B3	Disconnected. The master workstation chose to send a DISC because of a conflict with the System Image file, or possibly because of excessive errors during transmission.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • whether there is a [Sys]<Sys> WSnnn>SysImage.Sys file at the master workstation for the workstation type selected nnn. The type is either 255 (the default) or whatever was selected with the T option on the menu • the cluster communications cables • the CPU board
B4	Bad checksum of System Image. The System Image file transferred from the master workstation is not a valid run file. Either the file is invalid, or the transmission was faulty or incomplete. Check: • whether the operating system of the cluster workstation is valid • the CPU board (7201 or cluster communications logic) • the operating system or Communications Input/Output Processor of the master workstation (for a crash)
B5	Read error. Excessive input/output errors while trying to read a bootstrap interface block.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the CPU board (7201 or cluster communications logic) • the cluster communications cables
B6	Read timeout. During a read operation, no response was received from the master workstation. Check: the operating system of the master workstation (for a crash)
B7	Write DMA count is bad. After completion of a write operation, it was found that the entire block was not sent. Check: the CPU board (7201 or 8257)
B8	Write timeout. A write operation did not properly go to completion. Check: the CPU board (7201, 8257, or 8253)

Status Code (hexadecimal)	Meaning/Possible Causes
B9	Bad bootstrap block format. A bootstrap block of an invalid length was received. Check: whether the format of the bootstrap file is correct
BA	DMA error. After initializing the DMA for a read or write, the 8257 DMA controller did not contain the same information that was written to it. Check: the CPU board (8257)
BB to CF	Reserved for future use.
E0	ROM checksum error. There is a bad ROM chip on the CPU board at device location 3H.
E1	RAM error. An error occurred during initialization of the bootstrap ROM work area. The address where the error occurred is shown on the video display, followed by the value written and the value read. Check: the CPU board

Status Code (hexadecimal)	Meaning/Possible Causes
E2	RAM write/read 0's error.
E3	RAM write/read 1's error.
E4	RAM write/read address error. An error occurred during the read/write RAM test. All 1's, all 0's, or the sum of DS and DI are written, read, and compared. The comparison failed. Check : • the insertion of the CPU board • the CPU board
E5	RAM address test error. An error occurred during the RAM addressing test. After completion of the RAM read/write address test, each RAM word should contain the sum of its own DS and DI. The RAM address test verifies that this is true. This error can be caused by a short or an always low address line causing different addresses to be written to the same RAM. It may also be caused by memory that picks up or drops bits when idle. Check: • the insertion of the CPU board • the CPU board

Status Code (hexadecimal)	Meaning/Possible Causes
E6	keyboard initialization error. An error occurred while the bootstrap ROM was initializing the hardware.
E7 to EF	Reserved for future use.

8 AWS-220/-230 WORKSTATION BOOTSTRAP STATUS CODES

INTRODUCTION

When the workstation is bootstrapped, it goes through diagnostic and bootstrapping routines, that are resident in the ROM of the CPU. When an error is detected by the bootstrap ROM, the error code appears on the video display. For E0h and E1h error codes only, the workstation beeps on and off five times and the error code appears on the keyboard LEDs. (An E0h error code indicates a bad ROM, and an E1h error code indicates a bad RAM.)

ERRORS DURING BOOTSTRAP OR DUMP

The communications bootstrap or dump routines do not stop to report an error if there is no activity on the RS-422 cluster communications line. This can occur when the cable to the master workstation is disconnected, when the master workstation crashes, or when the master workstation is disabled by the Disable Cluster utility. When the connection with the master workstation is reestablished, the bootstrap or dump routine automatically starts (indicated on the video display by a period (.) for every sector transferred).

INTERPRETING KEYBOARD CODES

The E0h and E1h error codes are displayed on the keyboard LEDs. OVERTYPE is the most significant and f10 is the least significant. They are interpreted as follows:

LED	Error E0h	Error E1h
OVERTYPE	on	on
LOCK	on	on
F1	on	on
F2	off	off
F3	off	off
F8	off	off
F9	off	off
F10	off	on

CODE LISTING

The error codes are listed in hexadecimal format below. There is also a list of possible causes for most of the errors. (The causes are listed with the most likely one first.)

For more information see

AWS-220, -230, -240, Hardware Manual

Status Code (hexadecimal)	Meaning/Possible Causes
00 to 02	Reserved for future use.
03	Timeout waiting for an interrupt after a seek command. The floppy disk controller did not interrupt the CPU after being issued a seek command. Check: O that the operator did not open the door of the floppy disk drive O the seating of the FDC and CPU boards on the motherboard
04	Data bit set. The data input/output bit of the floppy main status register (port 80h bit 6) is continually set to 1. The CPU cannot issue a command to the floppy disk controller. Check: The FDC board (8272).

Status Code (hexadecimal)	Meaning/Possible Causes
05	Data bit not set. The request for master bit of the floppy main status register (port 80h bit 7) is never set to 1. The floppy disk controller can neither accept a data byte from the bus master nor send a byte to the bus master. Check: the FDC board (8272)
06	DMA not done. The byte count register of the 8257 channel 0 never decremented to 0, which means that the DMA operation never finished. Check: the CPU board (8257)
07 to 08	Reserved for future use.
09	Run file checksum error.
OA	File header invalid. The system image file on the floppy disk in drive 0 does not contain a valid run file. Since the Initialize Volume utility does not automatically copy a system image file onto the volume it is initializing, the user must copy a valid system image file onto the volume.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: the floppy disk
0B	Floppy control register inconsistent. The floppy main status register was polled until it became ready (Port 80h was 80h). The floppy main status register was then polled again and it was not ready. Check: the FDC board (8272)
0C	Floppy disk drive became not ready during a seek. The floppy disk drive became not ready while performing a Seek command. This error can be caused by opening the door of the floppy disk drive or by a bad cable from the floppy disk drive to the motherboard. Check: • operator intervention • the cable from the floppy disk drive to the motherboard • the floppy disk drive • the FDC board (8272)

Status Code (hexadecimal)	Meaning/Possible Causes
0D	Invalid floppy disk drive controller command received. The floppy disk drive controller received an undefined command during a Seek and Recalibrate command. Check: • the seating of the FDC board on the motherboard • the FDC board (8272)
0E	Floppy disk drive not ready. The floppy disk drive was not ready when the Seek or Recalibrate command was issued. Check: • that the floppy disk is inserted in drive 0 with the disk label on the opposite side of the release latch • that the door of the floppy disk drive is properly closed
0F	Floppy disk drive fault condition during a Seek or Recalibrate command. The floppy disk drive did not recalibrate to track 00 after 77 step pulses or the drive fault line went active.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the cable between the floppy disk drive and the motherboard • the floppy disk drive • the FDC board (8272)
10	Abnormal termination of Seek command. The floppy disk drive did not complete the Seek command correctly. Either the floppy disk drive failed or the ready status changed. Check: • operator intervention • the floppy disk • the cable between the floppy disk drive and the motherboard, • the floppy disk drive • the FDC board (8272)
11	Floppy disk drive became not ready. The floppy disk drive became not ready during a data transfer. This error is usually caused by opening the door of the floppy disk drive.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • operator intervention • the floppy disk • the cable between the floppy disk drive and the motherboard, • the floppy disk drive • the FDC board (8272)
12	Invalid floppy disk drive command received. The floppy disk drive controller reported an undefined command when the bootstrap ROM requested a data transfer. Check: • the seating of the FDC board on the motherboard • the FDC board (8272)
13	Floppy disk drive not ready. The floppy disk drive was not ready when a Read or Write command was issued. This error can occur only if the floppy disk drive was ready during a previous Recalibrate command and a previous Seek command. Check: operator intervention

Status Code (hexadecimal)	Meaning/Possible Causes
14	Floppy disk drive fault condition during a data transfer. The floppy disk drive's fault line went active. Check: • the cable between the floppy disk drive and the motherboard • the floppy disk drive
15	End of track. After a Read or Write command no EOT signal was received form the 8257 Check: • the cable between the floppy disk drive and the motherboard • the CPU board (8257) • the FDC board (8272)
16	Data error (data field). The floppy disk drive controller cannot read data from the floppy disk drive correctly. Check: • the floppy disk • the cable between the floppy disk drive and the motherboard • the floppy disk drive • the FDC board (8272)

Status Code (hexadecimal)	Meaning/Possible Causes
17	Data error (identification field). The floppy disk drive controller cannot read the identification field of the addressed sector. Check: • the floppy disk • the cable between the floppy disk drive and the motherboard • the floppy disk drive • the FDC board (8272)
18	Data late. The floppy disk drive controller did not get service from the 8257 in time. Check: • the seating of the CPU and FDC boards on the motherboard • the CPU board (8257) • the FDC board (8272)
19	No data (wrong track). During a Read or Write command, the floppy disk drive was on the wrong track. That is, either the floppy disk is incorrectly initialized or a Seek command sent the read/write head to the wrong track.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the floppy disk • the cable between the floppy disk drive and the motherboard • the floppy disk drive • the FDC board (8272)
1A	No data (bad track). The track accessed was marked as number 255 (0FFh). Check: • the floppy disk • the FDC Board (8272)
1B	No data. The floppy disk drive controller reported a no data condition. The specified sector could not be found. Check: • the floppy disk • the cable between the floppy disk drive and the motherboard • the floppy disk drive • the FDC board (8272)

Status Code (hexadecimal)	Meaning/Possible Causes
1C	Floppy disk write protected. This error code appears only during the dump operation and indicates that the floppy disk has a write protect tab in place. Check: the floppy disk
1D	Missing address mark (data field). The floppy disk drive controller cannot find any identification a address marks on the track. Usually, this error means that the floppy disk was not initialized by the Initialize Volume utility. Check: • the floppy disk • the cable between the floppy disk drive and the motherboard • the floppy disk drive • the FDC board (8272)
1E	Reserved for future use.
1F	Abnormal termination of command. The floppy disk drive controller reported abnormal termination of a command without reporting the cause. Check: the FDC board (8272)

9 AWS-240/COLOR WORKSTATION BOOTSTRAP STATUS CODES

INTRODUCTION

When the workstation is bootstrapped, it goes through diagnostic and bootstrapping routines, that are resident in the ROM of the CPU. When an error is detected by the bootstrap ROM, the error code appears on the video display. For E0h and E1h error codes only, the workstation beeps on and off five times and the error code appears on the keyboard LEDs. (An E0h error code indicates a bad ROM, and an E1h error code indicates a bad RAM.)

ERRORS DURING BOOTSTRAP OR DUMP

The communications bootstrap or dump routines do not stop to report an error if there is no activity on the RS-422 cluster communications line. This condition can occur when the cable to the master workstation is disconnected, when the master workstation fails, or when the master workstation is disabled by the Disable Cluster utility. When the connection with the master workstation is reestablished, the bootstrap or dump routine automatically starts (indicated on the video display by a period (.) for every sector transferred).

INTERPRETING KEYBOARD CODES

The E0h and E1h error codes are displayed on the keyboard LEDs. OVERTYPE is the most significant and f10 is the least significant. Interpret them as follows:

LED	Error E0h	Error E1h
OVERTYPE	on	on
LOCK	on	on
Fl	on	on
F2	off	off
F3	off	off
F8	off	off
F9	off	off
F10	off	on

CODE LISTING

The error codes are listed in hexadecimal format below. There is also a list of possible causes for most of the errors. (The causes are listed with the most likely one first).

For more information see

AWS-220, -230, -240 Hardware Manual

AWS Color Workstation Hardware Manual

Status Code (hexadecimal)	Meaning/Possible Causes
20 to 22	Reserved for future use.
23	Timeout waiting for an interrupt after issuing a Read or Write command. The disk controller did not interrupt the CPU after performing a Read or Write command. Check: • that the operator did not open the door of the floppy disk drive • the seating of the HDC and CPU boards on the motherboard
24	CMDBUSY always set. Bit 5 of Flag register 1 (port 8Eh) is continually set, which means that the disk controller cannot accept a command. Check: the HDC board

Status Code (hexadecimal)	Meaning/Possible Causes
25	STRDY never set. Bit 1 of Flag register 0 (port 8Fh) is never set, which means that the status registers cannot be read. Check: the HDC board
26	DMA not done. The byte count register of the 8257 channel 0 never decremented to 0. This means that the DMA operation never finished. Check: the CPU board (8257)
07 to 08	Reserved for future use.
29	Run file checksum error.
2A	File header invalid. The System Image file on the floppy disk in drive 0 does not contain a valid run file. Since the Initialize Volume utility does not automatically copy a System Image file onto the volume it is initializing, the user must copy a valid system image on the volume. Check: the floppy disk
2B	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
2C	Invalid command received. The disk controller received an undefined command from the host processor. Check: the seating of the HDC and CPU boards on the motherboard
2D	Drive not ready. The disk drive was not ready when a Seek or Recalibrate command was issued. Check: the disk drive power connections
2E	Disk fault condition during Fault or Recalibrate command. The disk drive did not recalibrate, or the drive fault line became active. Check: • the disk drive cable to the motherboard • the disk drive
2F	Abnormal termination of Seek command. The disk drive did not successfully seek a specified track. Either the drive failed or the ready status changed.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the disk drive cable • the disk drive • the HDC board
30	Disk drive became not ready. The disk drive became not ready during a data transfer. Check: • the disk drive cable • the disk drive • the HDC board
31	Invalid command (bad head). See 34 below for explanation.
32	Invalid command (bad sector). See 34 below for explanation.
33	Invalid command (bad track). See 34 below for explanation.
34	Invalid disk command issued. This explanation applies to codes 31 through 34. The disk controller received an invalid parameter or an undefined command from the CPU.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the disk drive cable • the HDC board • the CPU board
35	Disk drive not ready. The disk drive became not ready when a Read or Write command was issued. This error can occur only if the disk drive was ready during execution of a previous Recalibrate and Seek command. Check: • the disk drive cable • the HDC board • the CPU board
36	Disk drive fault condition during input/output. The disk drive fault line went active. Check : • the disk drive cable • the disk drive
37	Data late. The drive controller did not receive service from the 8257 DMA channel in time to satisfy the disk drive. This error code can only occur in reference to drive 0 on the AWS-240.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the floppy disk drive cable • the HDC board • the CPU board (8257)
38	Data CRC. See 39 for explanation.
39	Identification CRC. A Cyclical Redundancy Check (CRC) error occurred in a sector of data read or in the address information of the sector (identification). This generally indicated an error on the disk media. Check: • the disk drive • the disk drive cable • the HDC board (data separator) • the CPU board
3A	Halt during execution. The disk controller received a Halt command during execution of another command. Check: • the disk drive cable • the HDC board • the CPU board

Status Code (hexadecimal)	Meaning/Possible Causes
3B	Sector not found. The sector in a Read or Write command was not found on the track. This can occur if neither a sector mark nor a matching sector number were found. Check: • the disk drive • the disk drive cable • the HDC board (data separator) • the CPU board
3C	Abnormal termination of command (no specified cause). The disk reported abnormal termination of a command without reporting any cause. Check: the HDC board
3D	Invalid hard disk parameters. The parameters returned by the disk controller for either the number of sectors per track or the number of tracks per head was zero. Check: the HDC board
3E	Disk write protect. A write operation was attempted to a write protected disk.

Status Code (hexadecimal)	Meaning/Possible Causes
3F to 40	Reserved for future use.
41 to 5E	These codes are for drive 1 (hard disk) on the AWS-240/color workstation and are the same, respectively, as the 21 to 3E error codes listed above.
5F to A2	Reserved for future use.
A3	Serial input/output error. The serial input/output initialization routine detected an error in the serial input/output communications controller chip. Check: the CPU board (7201)
A4	8253 error. The clock initialization routine detected an error in the 8253 programmable counter/timer chip. Check: the CPU board (8253)
A5	No SIM. RIM was sent to the master workstation, but no SIM was received. This indicates that the workstation is able to receive but not transmit, or that the master workstation is able to transmit but not receive.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A6	No UP in initialization (SNRM). A UA or XID was sent to acknowledge the SIM sent by the master workstation, but the master workstation sent back an SNRM instead of a UA. The master workstation probably timed out while waiting for the UA or XID Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A7	No UP in initialization (DISC). A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back a DISC instead of a UA.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A8	No UP in initialization. A UA or XID was sent to acknowledge the SIM sent by the master workstation. The master workstation sent back something other than a UA. Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
A9	No identification available. The initialization routine monitored the cluster communications line but never found a free identification number. This is usually caused by attaching more workstations to a cluster communications line than the operating system of the master workstation is designed to accept. Check: the operating system of the master workstation, which may have crashed

Status Code (hexadecimal)	Meaning/Possible Causes
AA	Identification failure. The initialization routine found free workstation identification numbers by monitoring the communications line, but errors were detected when it tried to use one. This is usually caused by a failure of the collision recovery algorithm and can be overcome by pressing the reset button on each of the back panels of the workstations that collided.
AB	Read identification timeout. The initialization routine timed out after waiting 10 seconds while monitoring the communications line for a workstation identification number. This error code is only generated after a number of unsuccessful reads. Check: • the CPU board (7201 and cluster communications logic) • the master workstation • the communications cable • the operating system of the master workstation (for a crash)
AC	Bad address (dump routine). The workstation identification number sent in a frame by the master workstation did not match the one expected.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the communications cable • the CPU board
AD	Disconnected (dump routine.) The master workstation sent a DISC because of excessive line or protocol errors or because of a conflict with the crash/dump file at the master workstation. Check: • that either the file [Sys] <Sys> WSnnn> CrashDump.Sys or [Sys] <Sys>WS>CrashDump.Sys at the master workstation exists • that the file is not in use by another workstation that is dumping • that the file is large enough • the communications cable • the CPU board
AE	No UP - SNRM. See B0 below for explanation.
AF	No UP - REJ. See B0 below for explanation.
B0	No UP. This explanation applies to codes AE, AF, and B0. After transmitting a dump block, an unexpected response was received from the master workstation.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • whether an IWS cluster workstation is using the fixed identification mode • the CPU board (7201)
B1	Read UI error. A bootstrap block (frame type UI) was expected, but another frame type was received.
B2	Read SNRM error. A bootstrap block (frame type UI) was expected, but a SNRM was received. Check: the CPU board (7201)
B3	Disconnected. The master workstation chose to send a DISC because of a conflict with the system image file, or because of excessive errors during transmission.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • that there is a [Sys] <Sys> WSnnn> SysImage.Sys file at the master workstation for the workstation type selected nnn. The type defaults to 253 for the AWS-240, to 254 for the AWS-220 and 230, or to whatever was selected with the T option on the menu. If [Sys]<Sys>WSnnn> SysImage.Sys cannot be found, the default system image file [Sys]<Sys>WS>SysImage.Sys is loaded. • the cluster communications cables • the CPU board
B4	Bad checksum of system image. The System Image file transferred from the master workstation is not a valid run file. Either the file is invalid, or the transmission was faulty or incomplete. Check: • whether the operating system of the cluster workstation is valid • the CPU board (7201 or cluster communications logic) • whether the communications input/output processor of the master workstation has crashed
B5	Read error. Excessive input/output errors occurred while the bootstrap interface block was being read.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the CPU board (7201 or cluster communications logic) • the cluster communications cables
B6	Read timeout. During a read operation, no response was received from the master workstation. Check: the operating system of the master workstation, which may have crashed
B7	Write DMA count is invalid. After completion of a write operation, the bootstrap ROM determined that the entire block was not sent. Check: the CPU board (7201 or 8257)
B8	Write timeout. A write timeout did not properly complete. Check: the CPU board (7201, 8257, or 8253)

Status Code (hexadecimal)	Meaning/Possible Causes
B9	Bad bootstrap block format. A bootstrap block of an invalid length was received. Check: whether the format of the bootstrap file is correct
BA	DMA error. After initializing the DMA channel for a Read or Write operation, the 8257 DMA controller did not contain the same information that was written to it. Check: the CPU board (8257)
BB to CF	Reserved for future use.
E0	ROM checksum error. There is a bad ROM chip on the CPU board at device location 3H. This error is displayed on the keyboard LEDs, not the video display (see "Interpreting Keyboard Status Codes," above).
E1	RAM error. An error occurred during initialization of the bootstrap ROM work area. This error is displayed on the keyboard LEDs, not the video display (see "Interpreting Keyboard Status Codes," above).

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: the CPU board
E2	RAM read and write 0's error. See E4 below for explanation.
E3	RAM read and write 1's error. See E4 below for explanation.
E4	RAM read and write address error. This explanation applies to codes E2, E3, and E4. An error occurred during the read and write RAM test. All 1's, all 0's, or the sum of DS and DI are written, read, and compared. The comparison showed that the DS and DI were not identical. The error display for E2, E3, E4, and E5 (below) is: E: E2 1000:675C 0000 0002 where E: E2 is the error code, 1000:675C is the hexadecimal address, 0000 is the expected value, and 0002 is the received value. Check: that the CPU board is correctly seated on the motherboard

Status Code (hexadecimal)	Meaning/Possible Causes
E5	RAM address test error.
	An error occurred during the RAM addressing test. After completion of the RAM read/write address test, each RAM word should contain the sum of its own DS and DI. The RAM address test verifies that this is true.
	This error can be caused by a short or an always low address line allowing different addresses to be written to the same RAM. It may also be caused by memory that picks up or drops bits when idle.
	Check:
	that the CPU board is correctly seated on the motherboard
E6	Keyboard initialization error.
	An error occurred while the bootstrap ROM was initializing the hardware.
E7 to EF	Reserved for future use.
	The F0-F9 errors are generated by the communications test (menu option C). They indicate problems with the cluster communications and DMA logic or that the cluster cable was still connected to the workstation when the test was started.
F0	Underrun transfer ready not set.
	Status bits transmit underrun and/or transmit buffer empty were not set after a reset.

Status Code (hexadecimal)	Meaning/Possible Causes
F1	CTS and/or DCD set. The status bits CTS and DCD were not set after the transmitter was enabled.
F2	Carrier not clear. DCD did not clear after the transmitter was disabled.
F3	DMA write receive not ready. A character was written using DMA to the transmit buffer, but no character was received in the receive buffer.
F4	DMA write data error. A character was written using DMA to the transmit buffer. The character received in the receive buffer does not match the one written.
F5	DMA write data error bits. A frame was written using DMA to the transmit buffer. Though all characters within the frame were received correctly, no end-of-frame (EOF) character was received in the receive file. This usually indicates a chip failure.
F6	Timeout waiting for DMA read ready. A character was written using programmed input/output to the transmit buffer, but no character was received in the receive buffer.

Status Code (hexadecimal)	Meaning/Possible Causes
F7	DMA read EOF not set. A frame was written using programmed input/output to the transmit buffer. Though all characters within the frame were received correctly, no end-of-frame (EOF) character was received in the receive file. This usually indicates a chip failure.
F8	DMA read data error. A character was written using programmed input/output to the transmit buffer. The character received in the receive buffer does not match the one written.
F9	Carrier set after DISC. The DCD is still set. The most probable cause of the problem is the cluster communications cable. Check: • whether the cluster communications cable connected to the workstation • the CPU board
FA to FF	Reserved for future use.

10 IWS WORKSTATION BOOTSTRAP STATUS CODES

INTRODUCTION

When the IWS workstation is bootstrapped, it goes through diagnostic, memory dump, and bootstrapping routines, which are resident in the ROM. These routines light LEDs on the I/O Memory board and on the keyboard. When an error is detected by the ROM program, that error code is displayed on eight keyboard LEDs: OVERTYPE (OT), LOCK (LK) , Fl, F2, F3, F8, F9, and F10. (OT indicates the most significant bit of the error code; F10, the least.)

When an error code is displayed on the workstation keyboard LEDs, the workstation beeper is cycled on and off. This cycling continues indefinitely if the bootstrap ROM program was entered from a CTOS operating system crash, five times if the bootstrap ROM was entered from power-up or a reset, and three times if a boot timeout error (40h) occurs.

Before performing each diagnostic test, the bootstrap ROM program displays the diagnostic test it is about to run on the six I/O Memory board LEDs, CR1 through CR6. If an error occurs during the test, the same LED pattern that is displayed on the keyboard LEDs F1, F2, F3, F8, F9, and F10 is left on the I/O Memory board. (CR1 through CR6 display the lower six bits of an error code.)

The I/O Memory board LEDs should only be examined if the workstation beeper is cycling or if the processor has stopped executing. If the error code shown on the I/O Memory board LEDs is different from the error code shown on the workstation keyboard, the I/O Memory board LEDs are more likely to be correct.

If the workstation beeper does not cycle and there has been no disk activity, the problem is probably with the processor or with power. If the beeper does not cycle and there has been disk activity, the problem could lie within the operating system or diagnostic being loaded; the beeper could be broken, or the I/O Memory board switches could be set improperly (SW2 on the I/O Memory board has a default setting of all switches ON).

USING PANEL TO DIAGNOSE AN ERROR

A peripheral CRT and keyboard can be connected to the workstation using an RS-232-C crossed cable assembly. (See the Peripherals Hardware Manual, Section 4, "Additional IWS Peripherals Hardware," subsection, "RS-232-C Serial Interface.") The CRT should be set up to be 300 baud even parity. The Panel debugger program can be entered by pressing the space bar (20h), the carriage return (0Dh), or the ESCAPE key (1Bh) on a dumb terminal.

> NOTE
>
> If the error code is 40h (boot timeout), the space bar entry to Panel debugger must be performed within five seconds after the error code is displayed, or the ROM program will continue trying to bootstrap.

The 8086 register CX is set up to contain the error code before Panel debugger is entered. If the error is a memory error, information related to the error is contained in registers DS, DI, SI, and BP, as follows:

Register	Contents
CX	Error code
DS	Segment base address of memory error
DI	Offset address of memory error
SI	Data written to memory
BP	Data read back from memory

If there is an error in RAM, the Panel debugger could be unreliable, as it uses RAM (0:1D0 to 0:1F0) for its stack, and uses its stack for internal argument passing and to save the values of the registers. (The Panel debugger saves flags and register values when it is entered and restores them when it is exited.) Note that the only valid values of DS when a memory error occurs are those in which the last three digits are 0, such as 0000h, 1000h, etc. This information can be used to measure the reliability of the Panel debugger. In the case of a memory Read/Write error (60h), the only valid values of SI are 0000h, FFFh, and (DS+DI). In the case of a memory addressing error (80h), SI can only be (DS-DI). Register DI ranges from 0000h to FFFEh and is always even.

ERROR CODE DISPLAY

The 2716 ROMs display their error codes on the six LEDs located on the I/O Memory board. The 2732s display their error codes on the eight keyboard LEDs described below. Both methods of error display are accompanied by the system speaker. It beeps three times for a boot timeout error and five times for a hardware error.

You can determine the ROM type by looking at the keyboard LEDs after pressing the RESET button. If the system has a 2732 ROM, it displays a 1 (the F10 key lights), then a 21h (the Fl and F10 keys light), and an A1 (the OVERTYPE, F1, and F10 keys light). All LEDs light at the end of a successful boot. There is no display during a boot if your system has a 2716; only error codes are displayed.

INTERPRETING KEYBOARD CODES

The error code displayed on the keyboard LEDs is Interpreted as an 8-bit value, with the following bit assignments:

LED	Bit
OVERTYPE (OT)	7 (most significant bit)
LOCK (LK)	6
Fl	5
F2	4
F3	3
F8	2
F9	1
F10	0 (least significant bit)

CODE LISTING

The error codes are listed in hexadecimal format below. There is also a list of possible causes for most of the errors. (The causes are listed with the most likely one first).

For more information see

IWS Peripherals Hardware Manual (SMD Version)

Status Code (hexadecimal)	Meaning/Possible Causes
00	No power or inoperative keyboard. If the beeper is cycling, the keyboard may be inoperative. If the keyboard is inoperative, the lower six bits of the error code are displayed on the I/O Memory board LEDs as described in the introduction.

Status Code (hexadecimal)	Meaning/Possible Causes
	If the beeper is not cycling and there is no disk activity, check the power. If there is disk activity, the problem may be with the program that was booted. Note that it can take as long as 5 minutes for a cluster workstation CTOS operating system to initialize if the master workstation is heavily loaded. Check: • the workstation power indicator • the cable from the keyboard to the workstation • the keyboard • the software in SysImage.Sys file
01	Starting floppy dump or boot. This is not an error. This code is displayed on the LEDs just before a dump or boot is started. It is left there until the dump or boot is successfully completed, or an error occurs.
02	No floppy disk controller. A timeout occurred when the ROM program tried to access the floppy disk controller port (port 72h). The DCI cable could be disconnected, or the floppy disk controller could be installed. In this case, the workstation should be powered down and up again to clear the error.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable connection (both ends) • the I/O Memory board • the CPU board
03	Floppy disk controller register did not become ready in 3 seconds. The sequencer in the floppy disk controller was never ready to be used (that is, port 72h was not 80h). There is probably no power to the disk controller or, as mentioned for 02h, the floppy disk controller could be installed. In this case the workstation should be powered down, and then up again. Check: • the power-on indicator • the floppy disk controller or SMD Controller board • the I/O Memory board • the CPU
04	Data-in bit set in command. The floppy disk controller was trying to send information to the processor while the processor was trying to send a new command to the controller. This error code usually means that the floppy disk controller received an invalid command. However, this error can also result from a defective or poorly connected DCI cable.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board • the CPU
05	Data-in not set in result. When the processor expected result information, none was available. This error is similar to error 03. Check: • the DCI cable • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board • the CPU
06	DMA not completed. At the end of a disk transfer, the 8237 DMA count register was not 0FFFFh. This condition indicates a DMA problem. The DCI cable and the boards listed below can also cause this error.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable • the CPU board • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board • the Video board
07	Volume home block checksum error. The first block of information read from the floppy disk into memory is invalid. This might be because the floppy disk in drive 0 was never processed by the Initialize Volume utility. This error might also occur because the floppy disk is defective, the DMA logic is storing the wrong data in memory, or the floppy disk controller is malfunctioning. Check: • the floppy disk • the DCI cable • the CPU board • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board

Status Code (hexadecimal)	Meaning/Possible Causes
08	No file on floppy disk. The Volume Home Block on the floppy disk in drive 0 has a length of 0 (for the SysImage.Sys in boot, and the Crashdump.Sys in dump) that contains the program to be booted. When the Initialize Volume utility processed the floppy, the number of pages for the file was zero. Check: the floppy disk
09	Run file checksum. See 0A below for explanation.
0A	File header invalid. The System Image file on the floppy disk in drive 0 does not contain a valid run file. You must copy a valid System Image file onto it. The Initialize Volume utility does NOT automatically copy a System Image file onto the volume it is initializing. Check: the floppy disk
0B	Floppy Disk Controller register inconsistent. The Floppy Disk Controller register was polled until it became ready (port 72h was 80h), but the next time it was polled it was not ready.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable • the floppy disk controller or SMD Controller board • the I/O Memory board • the CPU board
0C	Floppy disk drive became not ready during Seek. The floppy disk drive went not ready while Seeking. Usually the operator causes this error by opening the door of the drive. Other causes are a bad floppy disk or a bad cable from the floppy disk controller to the drive. Check: • the floppy disk drive • the disk drive cable • the floppy disk controller or SMD Controller board
0D	Invalid floppy disk command received. This error code occurs when the floppy disk controller receives an undefined command during the Seek/Recalibrate phase. It is usually caused by a defective DCI cable rather than a defective floppy disk controller.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable • the floppy disk controller or SMD Controller board • the I/O Memory board
0E	Floppy disk drive not ready. The floppy disk drive was not ready when the Seek or Recalibrate command was issued. Check: • that the floppy disk is in drive 0 • that the floppy disk label is on the side opposite the release latch • that the door is closed properly
0F	Floppy disk drive fault condition during Seek/Recalibrate. This floppy disk drive failure occurs when the floppy disk does not Recalibrate after 77 step pulses, or when the drive fault line goes active. Check: • the floppy disk drive • the disk drive cable

Status Code (hexadecimal)	Meaning/Possible Causes
10	Abnormal termination of Seek. If the floppy disk did not finish a Seek correctly, the drive could be defective or the ready status could have changed. Check: • the operator • the floppy disk • the floppy disk drive • the Floppy Disk Controller board of the SMD Controller board
12	Invalid floppy disk command received. This error occurs if the floppy disk controller receives an undefined command when the ROM requests a data transfer. It could be due to a defective DCI cable. Check: • the DCI cable • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board

Status Code (hexadecimal)	Meaning/Possible Causes
13	Floppy disk drive not ready. This error can occur only if the floppy disk was ready during a previous Recalibrate and Seek. It is caused by the floppy disk drive not being ready when the Read or Write command is issued. The most likely cause for this error is removing the floppy disk after the bootstrap sequence has started. Check: the operator
14	Floppy disk fault condition during data transfer. Floppy disk drive fault line went active. Check: • the floppy disk drive • the disk drive cable
15	End of cylinder. After a Read or Write, no EOP signal is received from the DMA logic. This error usually indicates either a DCI problem or a DMA problem.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable • the 8237 CPU • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board
16	Data error: data field. The floppy disk controller was unable to read data from the floppy disk correctly. Usually the floppy disk is defective. Other possible causes are the disk cable or the floppy disk controller. Check: • the floppy disk • the floppy disk drive • the disk drive cable • the Floppy Disk Controller board or the SMD Controller board
17	Data error: ID field. The floppy disk controller was unable to read the ID of the addressed sector. Usually the floppy disk is defective. Other possibilities are the disk drive cable or the floppy disk controller.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the floppy disk • the floppy disk drive • the disk drive cable • the Floppy Disk Controller board or the SMD Controller board
18	Data late. The floppy disk controller did not get service from the DMA chip in time for the floppy disk. Check: • the 8237 CPU • the DCI cable • the Floppy Disk Controller board or the SMD Controller board • the I/O Memory board • the Video board
19	No data: wrong cylinder. During a Read or Write operation, the floppy disk was on the wrong cylinder. That is, either the floppy disk was initialized incorrectly or a Seek went to the wrong place.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the floppy disk • the floppy disk drive • the disk drive cable • the Floppy Disk Controller board or the SMD Controller board
1A	No data: bad cylinder. The cylinder accessed is marked as number 255 (0FFh). Check: • the floppy disk • the Floppy Disk Controller board and the SMD Controller board
1B	No data. The floppy disk controller reported a no data condition. This means that the specified sector could not be found. Most likely, the floppy disk is defective. Check: • the floppy disk • the floppy disk drive • the disk drive cable • the Floppy Disk Controller board or the SMD Controller board

Status Code (hexadecimal)	Meaning/Possible Causes
1C	Floppy disk write protected. This error is never sent to the keyboard LEDs because it can only occur in the dump when the floppy is being written to.
1D	Missing address mark: data field. The floppy disk controller was unable to find the data address mark of a sector. This usually means that the floppy disk is bad. Check: • the floppy disk • the floppy disk drive • the disk drive cable • the Floppy Disk Controller board or the SMD Controller board
1E	Missing address mark: ID field. The floppy disk controller was unable to find any ID address mark on a track. Usually this is because the floppy disk has not been initialized by the Initialize Volume utility. Check: • the floppy disk • the floppy disk drive • the disk drive cable • the Floppy Disk Controller board or the SMD Controller board

Status Code (hexadecimal)	Meaning/Possible Causes
1F	Abnormal termination of command (no specified cause). The floppy disk controller reported abnormal termination of a data command without reporting any cause. Check: the Floppy Disk Controller board or the SMD Controller board
20	ROM checksum error. There is a bad ROM chip on the CPU board (location F14 or F15). Check: CPU Board (2716 or 2732 ROMs)
21 to 2B	Same as 01 to 0B. These error codes are for Hard Disk unit 0. They are the same as those for the floppy disk, except that the controller is the Hard Disk Controller board (or SMD Controller board), and the Control register is port 7Ah.
2C	Invalid Hard Disk command received. The disk controller thinks that it has received an undefined command from the processor. Usually this is due to a defective DCI cable.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the DCI cable • the Hard Disk Controller board or the SMD Controller board • I/O Memory board • the 8237 CPU
2D	Drive not ready. The disk drive (unit 0) was not ready when the Seek or Recalibrate command was issued. Check: power indicator on disk drive
2E	Hard Disk fault condition during Seek/Recalibrate. Hard Disk drive (unit 0) failure. The drive did not Recalibrate after 77 step pulses or the drive fault line goes active. Check: • the Hard Disk drive • the disk drive cable
2F	Abnormal termination of Seek. This error indicates that the Hard Disk did not finish a Seek correctly. Either the drive (unit 0) failed or the ready status changed.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the Hard Disk • the Hard Disk drive • the disk drive cable • the Hard Disk Controller board or the SMD Controller board
30	Unit became not ready. The Hard Disk drive (unit 0) went not ready during a data transfer. Check: • the Hard Disk drive • the Hard Disk drive cable • the Hard Disk Controller board or the SMD Controller board
31	Invalid command: bad head. See 34 below for explanation.
32	Invalid command: bad sector. See 34 below for explanation.
33	Invalid command: bad cylinder. See 34 below for explanation.

Status Code (hexadecimal)	Meaning/Possible Causes
34	Invalid Hard Disk command issued. This explanation applies to codes 31 through 34. The Hard Disk controller thinks it received an illegal parameter or an undefined command from the processor. This error is usually due to a bad DCI cable. Check: • DCI cable • the Hard Disk Controller board or the SMD Controller board • the I/O Memory board
35	Drive not ready. The disk drive (unit 0) was not ready when the Read or Write command was issued. This error can occur only if the disk was ready during a previous Recalibrate and a previous Seek, and then went not ready. Check: • the DCI cable • the Hard Disk Controller board or the SMD Controller board • the I/O Memory board

Status Code (hexadecimal)	Meaning/Possible Causes
36	Hard Disk fault condition during I/O. Hard Disk drive (unit 0) failure. The drive fault line goes active. Check: • the DCI cable • the Hard Disk drive
37	Data late. The Hard Disk controller did not get service from the DMA chip in time to satisfy the Hard Disk. Check: • the 8237 CPU • the DCI cable • the Hard Disk Controller board or the SMD Controller board • the I/O Memory board
38	Data CRC. See 39 below for explanation.
39	ID CRC. A Cyclical Redundancy Check (parity error) occurred in a sector read (for a data CRC), or in the address information of the sector (for an ID CRC) . This generally means an error on the Hard Disk (unit 0).

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the Hard Disk • the data separator (on the Floppy Disk Controller board) • the disk drive cable • the Hard Disk Controller board or the SMD Controller board
3A	Halt during execution. The Hard Disk controller received a Halt command during execution of some other command. Usually this is due to a bad DCI cable. Check: • the DCI cable • the Hard Disk Controller board or the SMD Controller board • the I/O Memory board • the 8237 CPU
3B	Sector not found. The sector in a Read or Write command was not found on the track (unit 0). This could be because no sector mark or no matching sector number was found.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the Hard Disk • the data separator (on the Floppy Controller board) • the disk drive cable • the Hard Disk Controller board or the SMD Controller board
3C	Abnormal termination of command (no specified cause). The Hard Disk reported abnormal termination of a data command without reporting any cause. Check: the Hard Disk Controller board or the SMD Controller board
3D	Invalid disk parameters. The parameters returned by the Hard Disk controller for either the number of sectors per cylinder or the number of cylinders per head were zero. Check: the Hard Disk Controller board or the SMD Controller board
3E to 3F	Reserved for future use.

Status Code (hexadecimal)	Meaning/Possible Causes
40	Boot timeout. If the boot program cannot find a floppy or Hard Disk that is ready and contains a System Image file before the communications routine times out (error code 0A2h), the program retries all devices. After four complete cycles, this error code is displayed, and the beeper sounds three times. This error code is displayed for 8 seconds. If a video terminal is attached and the correct character is typed on the keyboard, the Panel debugger can be entered; otherwise the program recycles. After each subsequent set of four cycles, the error code is displayed for 5 seconds, but the beeper does not sound again. The error codes that may be reported as 40h are 02h, 22h, 42h, 62h, 82 (no DCR); 08h, 28h, 48h, 68h, 88h, (unit has no System Image file); 0Eh, 2Dh, 4Dh, 6Dh, 8Dh (unit not ready); and 0A2h (workstation never polled).
41 to 5F	Same as 21 to 3F. These error codes are for disk unit 1; they are the same as those for disk unit 0.
60	RAM Read/Write test error. An error occurred during the Read/Write RAM test; all one, all zeros, and the sum of DS and DI were written and then read and compared. This error code indicates that the comparison failed.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • I/O Memory board insertion • I/O Memory board • the 8237 CPU
61 to 7F	Same as 21 to 3F. These error codes are for disk unit 2; they are the same as those for disk unit 0.
80	RAM address test error. An error occurred during the RAM addressing test. After the completion of the RAM Read/Write test, each RAM word must contain the sum of its own DS and DI. The RAM address test verifies that this is true. This error can result from a short that causes data for different addresses to be written to the same RAM. It can also be caused by memory that picks up or drops bits when idle. Check: • I/O Memory board insertion • the I/O Memory board • the 8237 CPU

Status Code (hexadecimal)	Meaning/Possible Causes
81 to 9F	Same as 21 to 3F. These error codes are for disk unit 3; they are the same as those for disk unit 0.
A0	Communications data transfer.
A1	Doing dump or boot. This code is displayed at the start of a dump or boot. It is left there until the master protocol is initialized or until an error occurs. Once the protocol is established, the codes 0A0h and 0A1h are shown alternately after every successful data transfer. This does not indicate any problem. This code is cleared at the end of the boot or dump procedure.
A2	Never polled. This indicates a nonfatal error and occurs when a disk waits 10 seconds for an initial poll from the master workstation. This error is reported during the boot initialization routine as part of error code 40h. It is never displayed in the LEDs of the keyboard. Check: • the communications cable • the I/O Memory board (SIO or RS-422 receivers) • that the master workstation operating system is running

Status Code (hexadecimal)	Meaning/Possible Causes
A3	SIO error. This error is shown when the SIO initialization routine detects an error in the SIO communications controller IC. Check: the I/O Memory board (SIO port)
A4	8253 error. The Clock Initialization routine detects an error in the programmable counter/timer 1C. Check: the I/O Memory board (8253)
A5	No SIM. A RIM was sent to the master workstation, but no answering SIM was received. This can indicate that the workstation is able to receive but not transmit, or that the master workstation is able to transmit but not receive. Check: • the I/O Memory board (SIO or RS-422 receivers/drivers) • the master workstation • the communications cable • the master workstation operating system (for a crash)

Status Code (hexadecimal)	Meaning/Possible Causes
A6	No UP in initialization (SNRM). A UA or XID was sent to acknowledge the SIM sent by the master, but the master sent back an SNRM instead of a UA. This is probably caused by the master timing out while waiting for the UA or XID. Check: • the I/O Memory board (SIO or RS-422 receivers/drivers) • the master workstation • the communications cable • the master workstation CTOS operating system (for a crash)
A7	No UP in initialization (DISC). A UA or XID was sent to acknowledge the SIM sent by the master, but the master sent back a DISC instead of a UA. The most likely cause is that switches are set for something other than fixed WsNumber mode, and the master workstation CTOS operating system is a version that is earlier than 5.0, which does not accept the XID as valid protocol.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • switch settings • the I/O Memory board (SIO or RS-422 receivers/drivers) • the master workstation • the communications cable • the master workstation operating system (for a crash)
A8	No UP in initialization. A UA or XID was sent to acknowledge the SIM sent by the master, but the master sent back something else instead of a UA. Check: • the I/O Memory board (SIO or RS-422 receivers/drivers) • the master workstation • the communications cable
A9	No ID available. The initialization routine listened to the communications line, but never found a free ID number. This is usually caused by attaching more workstations to a line than the master workstation operating system can handle. Check: the master workstation operating system (for a crash)

Status Code (hexadecimal)	Meaning/Possible Causes
AA	ID failure. The initialization routine found free ID numbers when it listened to the communications line, but errors were detected every time it tried to use a number. This error is usually due to a failure of the collision recovery algorithm. It can be overcome by pressing the reset button on the stations that have collided.
AB	Read ID timeout. The initialization routine timed out after 10 seconds while listening to the communications line for an ID number. This error is generated only after some number of successful reads. Check: • the I/O Memory board (SIO or RS-422 receivers/drivers • the master workstation • the communications cable • the master workstation operating system (for a crash)
AC	Bad address (dump routine). This error occurs when the workstation ID sent in a frame by the master workstation does not match the one expected. This error is never displayed on keyboard LEDs because the program continues to do a memory test and then boot.

Status Code hexadecimal)	Meaning/Possible Causes
AD	Disconnected (dump routine). The master workstation sends a DISC because of excessive line or protocol errors, because there is no file to which to write the memory dump, or because the file is not large enough for the entire dump. This error is never displayed on keyboard LEDs because the program continues to do a memory test and then boot.
AE	No UP: SNRM. See B0 below for explanation.
AF	No UP: REJ. See B0 below for explanation.
B0	No UP. This explanation applies to codes AE, AF, and B0. After the dump block was transmitted, an unexpected response was received from the master workstation. These errors are never displayed on keyboard LEDs because the program continues to do a memory test and then boot.
B1	Read UI error. A bootblock (frame type UI) is expected, but another frame type is received.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the I/O Memory board • that there is not a duplicate workstation ID
B2	Read SNRM error. A bootblock (frame type UI) is expected, but an SNRM is received. Check: the I/O Memory board (SIO)
B3	Disconnected. The master workstation decides to send a DISC due to excessive errors during transmission. This may be caused by having several workstations in the fixed WsNumber mode with the same switch settings. Check: • the communications cables • the I/O Memory board (SIO or RS-422 transmitters) • workstation IDs in fixed WsNumber mode (duplicate IDs)
B4	Bad checksum of system image. The System Image file transferred from the master workstation is not a valid run file. Either the file is invalid, or the transmission was faulty or incomplete.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • cluster workstation operating system file validity • that there are not duplicate workstation IDs (fixed WsNumber mode) • the I/O Memory board (SIO or RS-422 receivers) • the communications cables • the master workstation operating system or IOP (for a crash)
B5	Read error. Excessive I/O errors occurred while trying to read a bootblock. Check: • the I/O Memory board (SIO or RS-422 receivers) • the communications cables
B6	Read timeout. During a Read operation, no response was received from the master workstation. Check: the master workstation operating system (for a crash)

Status Code (hexadecimal)	Meaning/Possible Causes
B7	Write DMA count bad. This error occurs after completion of a Write operation if the entire block has not been sent. Check: • the I/O Memory board (SIO) • the 8237 CPU
B8	Write timeout. A Write operation did not properly go to completion. Check: • the 8273 CPU • the I/O Memory board (SIO or 8253)
B9	Bad bootblock format. An illegal length bootblock was received. Check: the boot file format
BA	DMA error. After initializing the DMA for a Read or Write operation, the 8237 DMA controller does not contain the same information as was written to it.

Status Code (hexadecimal)	Meaning/Possible Causes
	Check: • the 8237 CPU • the I/O Memory board • the video board
BB to FE	Reserved for future use.
FF	Successful boot. This is not an error. This code is displayed on the keyboard LEDs for one second just before the bootstrap ROM jumps into the program that it loads.

APPENDIX A: ACRONYMS

The following acronyms are used throughout this manual.

Acronym	Meaning
ACTLU	Activate Logical Unit
AP	Application Processor
ARIB	Active Runfile Information Block
ASIB	Active State Information Block
BCD	Binary Coded Decimal
BGP	Business Graphics Package
BSC	Binary Synchronous Communications
BSWA	Byte Stream Work Area
CGM	Computer Graphics Metafile
CLCB	Communications Line Configuration Block
CNM	Communication Network Manager
CPU	Central Processing Unit
CP	Cluster Processor
CR	Carriage Return
CRC	Cyclical Redundancy Check
CRT	Cathode Ray Tube
CS	Code Segment
CTS	Clear To Send

Acronym	Meaning
CWS	Cluster Workstation
DAM	Direct Access Method
DAWA	Direct Access Work Area
DCB	Device Control Block
DCD	Data Carry Detect
DCE	Data Communications Equipment
DCI	Disk Controller Interface
DFC	Data Flow Control
DIO	Data Input/Output
DISC	Disconnect
DLE	Data Link Escape
DMA	Direct Memory Access
DP	Data Processor
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTMF	Dual Tone Multifrequency
ECC	Error Correction Code
EOF	End-Of-File or End-Of-Frame
EOM	End Of Medium
EOP	End Of Process
EOT	End Of Transmission
ERC	Error Code
FAB	File Area Block

Acronym	Meaning
FAM	Folder Access Method
FDC	Floppy Disk Controller
FHB	File Header Block
FIFO	First In, First Out
FP	File Processor
GPAM	Generic Print Access Method
GPAMWA	Generic Print Access Method Work Area
GPS	Generic Print System
HDC	Hard Disk Controller
HDLC	High Level Data Link Control
LF	Line Feed
ICMS	Inter-Context Message Server
IOB	Input/Output Block
IP	Instruction Pointer
IRR	Interrupt Request Register
ISR	Interrupt Service Routine
ISAM	Indexed Sequential Access Method
ISR	Interrupt Service Routine
KDS	Kernel Data Segment
LCN	Logical Channel Number
LED	Light-Emitting Diode
LU	Logical Unit
ME	Memory Expansion

Acronym	Meaning
MFD	Master File Directory
MP	Master Processor (this can be a Data Processor or File Processor)
MLU	Multiple Logic Unit
MPU	MultiPhysical Unit
NBS	National Bureau of Standards
NMI	Nonmaskable Interrupt
NRZI	Non-Return to Zero Invert
PCB	Process Control Block
PDN	Public Data Network
PIT	Programmable Interval Timer
PLU	Primary Logical Unit
PROM	Programmable Read Only Memory
PU	Physical Unit
PVC	Permanent Virtual Circuit
QIC	Quarter-Inch Cartridge
RAM	Random Access Memory
RCB	Request Control Block
RD	Request Disconnect
RIM	Request Initialization Mode
RJE	Remote Job Entry
RNR	Recovery Not Ready
ROD	Regional Overlay Descriptor

Acronym	Meaning
ROM	Read Only Memory
RQR	Request Recovery
RSAM	Record Sequential Access Method
RSWA	Record Sequential Work Area
RTC	Real Time Clock
SC	Storage Controller
SDLC	Synchronous Data Link Control
SIO	Serial Input/Output
SIM	Set Initialization Mode
SNA	System Network Architecture
SNRM	Set Normal Response Mode
SP	Storage Processor
SPA	System Performance Accelerator
SRP	Shared Resource Processor
SSCP	System Services Control Point
STAM	Standard Access Methods
SVC	Switched Virtual Circuit
TIB	Task Information Block
TP	Terminal Processor
TPDU	Terminal Protocol Data Unit

Acronym	Meaning
TSAP	Transport Service Access Point
UA	Unnumbered Acknowledge
UCB	User Control Block
UI	Unnumbered Data Frame
UP	Unnumbered Poll
VAM	Video Access Method
VC	Virtual Circuit
VCB	Video Control Block or Virtual Control Block (when used in CT-Net X.25 Media)
VDM	Video Display Management
VHB	Volume Home Block
VLPB	Variable Length Parameter Block
VM	Virtual Memory
VTI	Virtual Terminal Interface
XID	Identification Frame

ETK-0010-T3

FUJITSU MINI-THERMAL PRINTER
40 CHARACTER: IN ACCORDANCE WITH CENTRONICS STANDARD
OPERATION INSTRUCTIONS
FTP-040UC

December, 1983

F U J I T S U L I M I T E D
Communications and Electronics
Marunouchi, Tokyo, Japan

TABLE OF CONTENTS

1. FEATURES 1

2. SPECIFICATIONS 3
   - 2.1 Configuration 3
   - 2.2 Character Printing 3
   - 2.3 Form Feed 4
   - 2.4 Interface Specifications 4
   - 2.5 Power Source 9
   - 2.6 Exterior Dimensions and Weight 9
   - 2.7 Print Form 10
   - 2.8 Environment Requirements 10

3. PRINTER FUNCTIONS 11
   - 3.1 Initialization 11
   - 3.2 Detecting Function 11
   - 3.3 Self Diagnosis Function 12
   - 3.4 Line Feed Function 13
   - 3.5 Control Codes 14

4. OTHERS 25
   - 4.1 Character Print Example 25
   - 4.2 Notes on Use 25
   - 4.3 Options 25

This document may be changed without prior notice.

1 FEATURES

Fujitsu mini thermal printer can print out very clear Graphic print. Because it is used the linje-dot print method with non movable. As the head print dots operating in close contact with the thermal forms, the resulting print is very clear and thermal contains no blurs. Also as printing is available by moving only the forms while its head being fixed, the printer noise generated by the head movement has been eliminated.

Along with this, the printing speed has been improved to 80 characters/sec which can also be applied to graphics. Maintenance is not necessary because it does not use ink ribbon and movable head. Moreover, it can be easily connected to the host as it is in accordance with the Centronics Standard. Application is for measuring instruments, personal computers, etc.; the mini-printer satisfies the long-cherished user needs with its multipurpose functions.

(1) Long life

The unique structure protects the print head from wear, providing an operating life of up to 20 million dot lines.

(2) High-speed printing

The FTP-040UC is with the average speed of 80 characters/sec averages 80 characters/sec.

(3) Clear printing

The fixed print head operating in stable contact with the thermal forms provides clear character and graphic printing.

(4) Quiet printing

The line-dot printing method provides quiet office environment even while printing.

(5) The Centronics Interface Standard

Easier connection with the host is available as the printer interface is in accordance with this general standard.

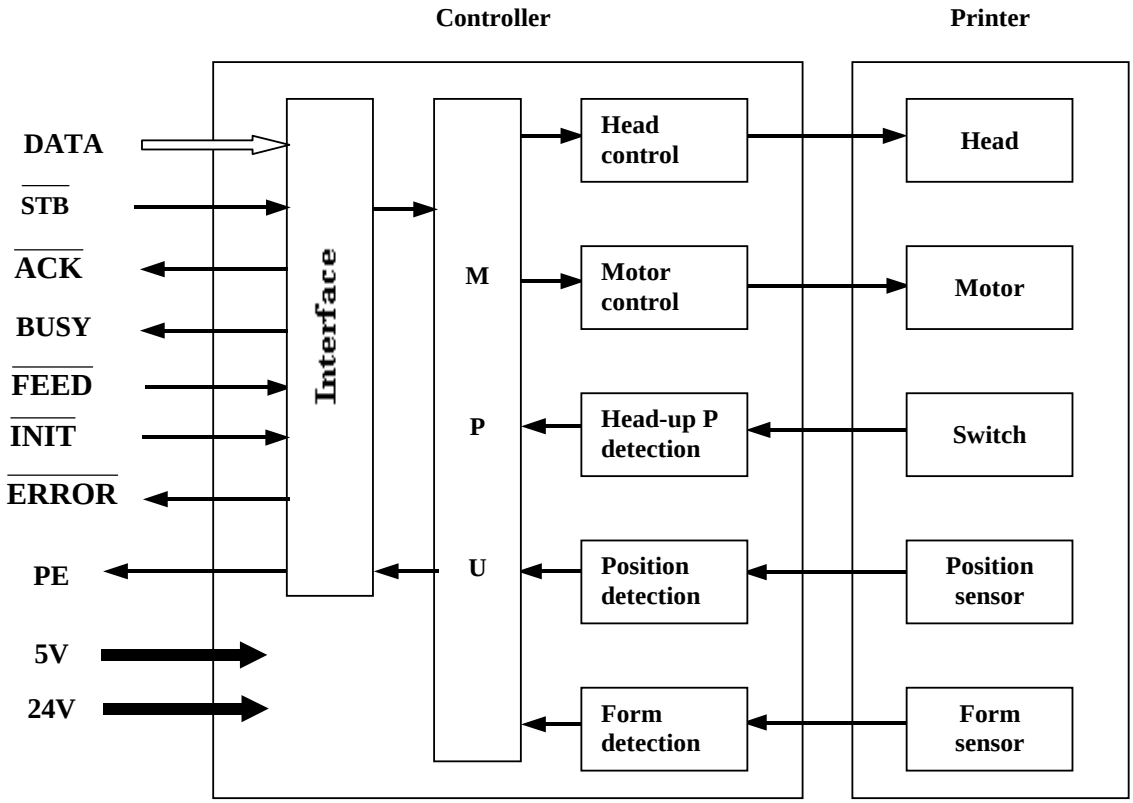
(6) Applications

The FTP-040UC is designed for use with personal computers, POS, and Car Faxsimiles, and also in measuring, analysis, and medical equipments.

2 SPECIFICATIONS

2.1 Configuration

The printer unit consists of the printer and the controller.



2.2 Character Printing

(1) Printing method : Thermal line-dot printing method

(2) Dot configuration : 280 line dots

(3) Dot pitch (Horizontal) : 2.8 dots/mm (70 dots/in.)

(4) Printing character : 40 characters

(5) Character size (character mode) : 1.8 (W) x 3 (H) mm (standard)
3.6 (W) x 3 (H) mm (enlarged)

(6) Character position : See Figure 1.

(7) Printing speed : 2 lines/sec
(standard: 80 characters/sec
enlarged: 40 characters/sec)

: 23 dot lines/sec - Graphic mode

(8) Character configuration : 5 x 7 dots - character mode
8 x 32 bits/line - graphic mode

(9) Character set : JISCII (160 characters)

(10) Printing life : Equivalent to or more than 2 million lines (20 millions dot lines)

2.3 Form Feed

(1) Feeding method : Friction feed

(2) Feeding pitch : 4.23 mm (1/6 in.) - character mode
Dot feeding pitch
0.42 mm (character mode)
Dot feeding pitch
0.36 mm (graphic mode)

2.4 Interface Specifications

(1) Input requirements

- o Input method : In accordance with the Centronics standard (8-bit parallel)
- o Transmission speed (min.) : 1000 CPS - character mode
2000 *BPS - graphic mode (* BYT)
- o Synchronization method : External strobe pulse
- o Handshaking : $\overline{\text{ACK}}$ /BUSY signal
- o Input/output level : TTL level

(2) Functions

- o Code table : See Table 1
- o Control code : See Table 2
- o Functions :

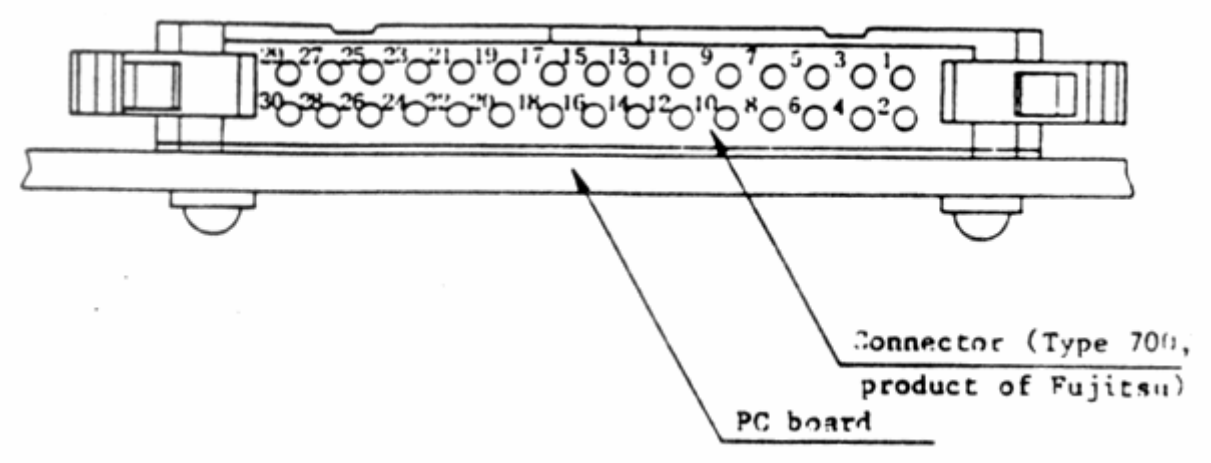
Enlarged printing
(doubled in the horizontal direction)
Reverse printing
Page length setting
—— Character mode only

Black and white reverse display
—— Graphic mode only

(3) Connector pin arrangement and contents

- o Arrangement

Pin No.	Signal name	Pin No.	Signal name
1	$\overline{\text{STB}}$	2	GND
3	DATA 1	4	"
5	" 2	6	"
7	" 3	8	"
9	" 4	10	"
11	" 5	12	"
13	" 6	14	"
15	" 7	16	"
17	" 8	18	"
19	$\overline{\text{ACK}}$	20	"
21	BUSY	22	"
23	PE	24	"
25	+5V	26	$\overline{\text{INIT}}$
27	NC	28	$\overline{\text{ERROR}}$
29	$\overline{\text{FEED}}$	30	GND



*: Use ECN-707B030-AU/B (product of Fujitsu) as the interface signal input connector.

*: The interface signal input cable should be 500 mm or less in 1ength (recommended).

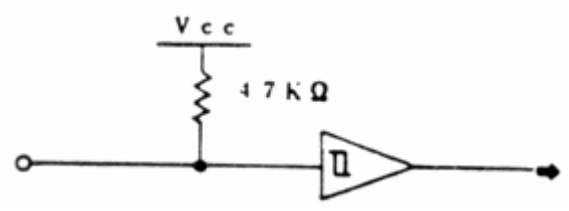
o Explanation of contents

Pin No.		Signal name	Direction	Explanation
1	2	$\overline{\text{STB}}$	IN	• Data read strobe signal • Pulse width must be 0.5 μsec or • Data is read when signal goes from High to Low.
3.5.7. 9.11. 13.15.17	4.6.8 10.12.14. 16.18.	DATA 1 to 8	IN	• S-bit parallel data • Active-high
19	20	$\overline{\text{ACK}}$	OUT	• Acknowledge pulse output at data input completion. • It may be data transmission request pulse. • Pulse width is approx. 10 μsec.

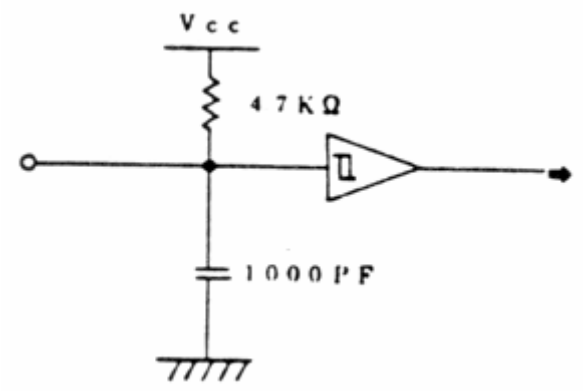
Pin No.		Signal name	Direction	Explanation
21	22	BUSY	OUT	• DC level signal indicating whether the printer is ready or not • Outputs a high level signal under the following conditions: ① During data entry ② When the print head is in up-position or no thermal print form is provided. ③ During forms feed
23	24	PE	OUT	• DC level signal indicated when head is up or no form is provided • Active-high
26		$\overline{\text{INIT}}$	IN	• Resets the printer to initial status. • 50 sec or more is required at the receiving end. • The BUSY signal become low level at 300 ms (maximum) after the INIT signal has been released.
28		$\overline{\text{ERROR}}$	OUT	• Outputs a Low level signal when the printer is under the following condition: ① When the printer head is in up-position or no form is provided
29	30	$\overline{\text{FEED}}$	IN	• After power is on, the buffer contents are printed and line feed operation is executed when signal goes Low (Pulse width equivalent to or more than 15 msec is required) • When signal has gone Low with power on, TEST printing is executed.

(4) Input / output requirements

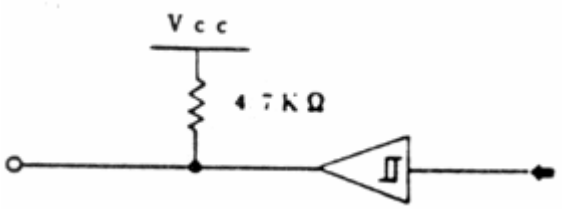
o DATA 1~8, $\overline{\text{FEED}}$, $\overline{\text{INIT}}$



o $\overline{\text{STB}}$



o BUSY, $\overline{\text{ACK}}$, PE, $\overline{\text{ERROR}}$



Note: Set Fanin and Fanout to logical 1, connect the 74 LS or equivalent to the host system, and install 4.7 - KΩ pull-up resistance as the terminator.

(5) Tuning chart

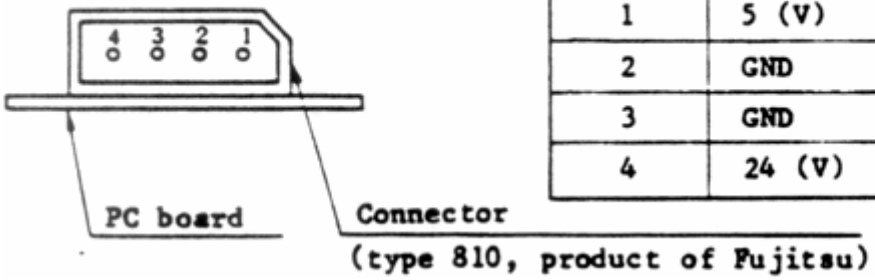
Figures 2 and 3 show the timing charts.

2.5 Power Source

(1) Voltage/current 5±5% (V) 1 (A) (max.)
24?% (V) 2.5 (A) (max.)

Note: The voltage identifies the terminal voltage at the power source connector.

(2) Pin arrangement



Pin No.	Contents	Cable color (*1)
1	5 (V)	Red
2	GND	Black
3	GND	Black
4	24 (V)	Orange

*1: The power source cable is attached (1m in length).

2.6 Exterior Dimensions and Weight

(1) Printer

- o Dimensions 134.5 (W) x 89 (D) x 48 (H) mm
- o Weight Approx. 500 g

(2) Controller

- o Dimensions 133 (W) x 163 (D) x 20 (H) mm
- o Weight Approx. 200 g

(3) Exterior appearance: See Figure 4.

2.7 Print Form

(1)	Form	: Thermal print form
(2)	Form width	: 110 mm.
(3)	Recommended form	: FTP-040P011 ... TP50KS-F(Jujo paper) : FTP-040P021 ... F-200H (Mitsubishi paper) : FTP-040P031 ... PS65B (Honshu Paper)

2.8 Environment Requirements

(1)	Operating ambient temperature	: 5癈(*1) ~ 50癈
(2)	Storage temperature	: -20癈(*1) ~ 60癈
(3)	Operating humidity	: Less than 40癈, 90% RH
(4)	Vibration resistance	: MIL-STD-202D, 201A (10G, approx. 2 hours in each of three directions at right angle)
(5)	Shock resistance	: MIL-STD-202D, 213B, A (50G, for 11 msec in six directions at right angle)
	*1	: No dew condensation is allowed.

3. PRINTER FUNCTIONS

3.1 Initialization

(1) Initialization mode

- o When power is turned ON or when power is turned ON again after being turned OFF, printer is initialized.
- o When INIT signal is applied to the interface connector, printer is initialized.

(2) After initialized, the printer is set in the following status:

- o Printer is automatically enabled to receive data unless it runs out of form or is set to head-up status.
- o Print buffer is cleared.
- o Number of lines per page is set to 35.
- o Line pitch is set to 1/6 inch.
- o Printer is set to normal standard character print mode.

3.2 Detecting Function

(1) Head-up detection

- o Detected status — Detects the condition in which the thermal head is not in contact with the form (the head-up lever is operated)
- o Operation — After the printer has printed 1 dot line, the motor is stopped and the printer operation is not restarted unless the head-up condition or no-form condition is recovered.

(2) Shortage of form detection

- o Detected status — When the printer is short of form, the shortage-of-form condition is detected.

- Operation — After the printer has printed 1 line in character print mode and 1 dot line in graphic print mode, the motor is stopped and the printer operation is not restarted unless the head-up condition or no-form condition is recovered.

  Note: The BUSY signal goes High when the head is up or no form is provided.

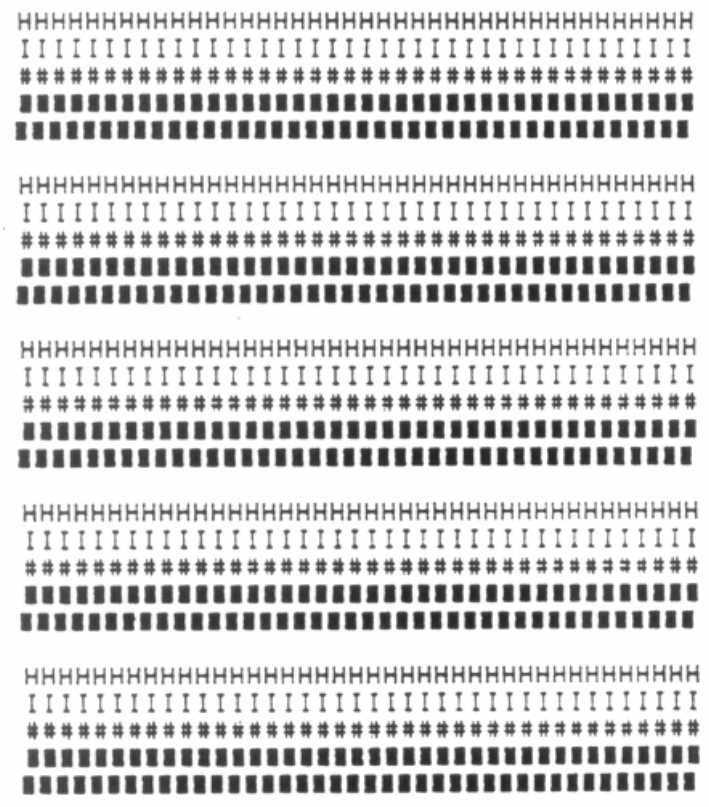
3.3 Self Diagnosis Function

This printer has a self diagnostic function which allows printing test patterns even if it is not connected to the host. This function enables to test the thermal head, print mechanism, and print quality.

< Method >
The self diagnosis function is enabled by turning on the power supply while pin 29 (FEED) of interface connector CN1 is connected to the GND level (pin 30, etc.), and continues operation until the printer runs out of form, head-up condition occurs, or the power is turned OFF.

This test function cannot be executed when the printer is out of form or in head-up condition even if the power has been turned ON.

< Printing example >



3.4 Line Feed Function

This printer has line feed function independent of the control code.

Line feed operation is executed when pin 29 (FEED) of interface connector CN1 is held at LOW level for 15 msec or more while the printer is in character code input status. At this time, the printer prints the buffer data and feeds a single line.

Note: Line feed function is ignored in graphic mode and when an escape command is entered.

3.5 **Control Codes** (those indicated by * are valid only in the character mode)

(1) CR* (carriage return)

CR code releases the double-width enlarged character print mode.

(2) LF* (Line feed)

LF code prints buffer data and feeds a single line.

- o If there is no print data previous to the LF code, that is, when the LF code is entered while the buffer is empty, the printer executes no print operation but feeds only one line.
- o When print data (including space) for all columns has been entered and the following data is also print data, or when 39-column data has been entered and the following data is double-width enlarged character data, the data in the print buffer is printed out automatically.

(3) FF* (form feed)

FF code prints out buffer data. It also positions the print starting point in the initial print position on the next page according to the initial setting (35 lines/page) or page length setting (ESC which will be described later).

- o The print starting point is set to the initial print position when the power is turned on, when INIT signal is applied to pin 26 of the interface connector, or when page length is set using the control code.
- o When no page length has been set, the default value is automatically 35 lines/page.
- o As the page counter does not operate in graphic print mode, the initial print position on a page shifts by the amount equal to graphic print dot line.

(4) SO* (shift out)

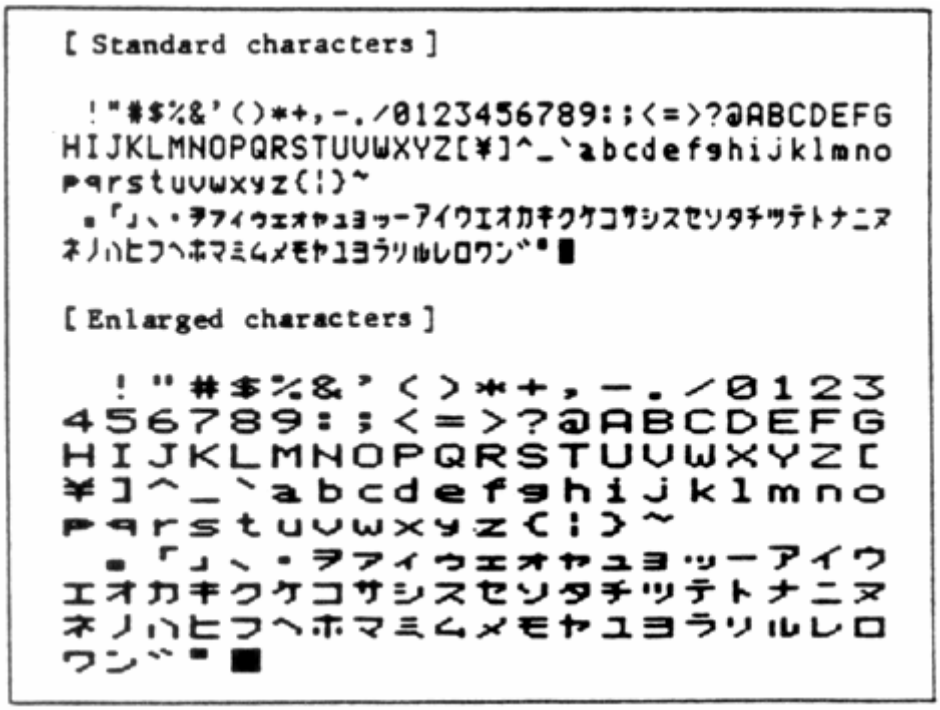
SO code prints the data remaining in the current line in double-width character print mode. This code may be entered at any print position in a line. This function can also be used in the same way in reversed character print mode. This mode is released by the CR or SI code.

When a line contains both standard and enlarged characters, the print buffer data is automatically printed when the enlarged character reaches the 40th character (calculated in terms of standard characters).

(5) SI* (shift in)

SI code releases double-width enlarged character print mode.

<Print example>



(6) RS (record separator)

After the RS code has been entered, input data is printed in on black-on-white-reverse-print mode when the printer enters graphic mode. This function is released by the US code.

(7) US (unit separator)

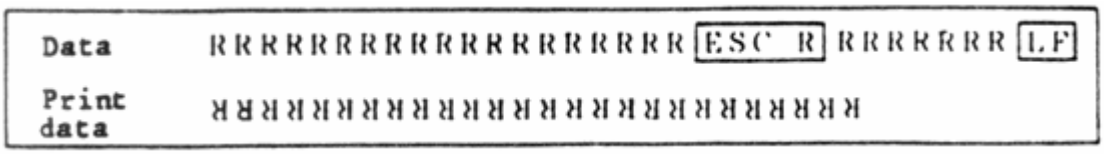
US code releases black-on-white-reverse-print mode.

(8) Escape alphabet control

① ESC R * [reversed character print function]

The [ESC R] code may be entered at any print position in a line. However, as reversed print operation is executed in line units, the data entered in the buffer prior to the [ESR R] code is also printed in the reverse mode if it is identical. [ESR R] code executes reversed print when the following [LF] code, [FF] code, or buffer full status activates buffer data print operation.

<Printing example>



② ESC S* (releasing reverse character print function)

This code releases reverse character print function.

③ ESC C + n * (setting page length)

This code is used to set page length (number of lines per page)

- The number of lines must be within the range from 1 to 256.
- Set n using two digits in hexadecimal numbers. 01H to 00H

<1> <256>

- When page length is not set, the default value is 35 lines per page.

④ ESC V * n1 + n2 (setting graphic mode)

The [ESC V] code and n1 and n2 following it set the printer to graphic mode.

This [ESC V] code is valid only in character mode. n1 and n2 following the[ESC V] code specify the number of dot lines for graphic printing. The number of graphic data portions actually transmitted is calculated as follows:

(number of graphic data portions) = (32 bytes) x (number of dot lines)

Therefore, when a printer receives graphic data corresponding to the number of dot lines specified in subscripts n1 and n2, it automatically resets itself to character mode and continues to receive character data.

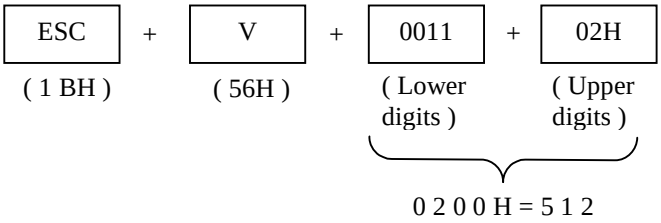
32 bytes of graphic data can be printed in one dot line when the [ESC V] code has been entered. The maximum number of print lines which can be set using subscripts n1 and n2 is 65536.

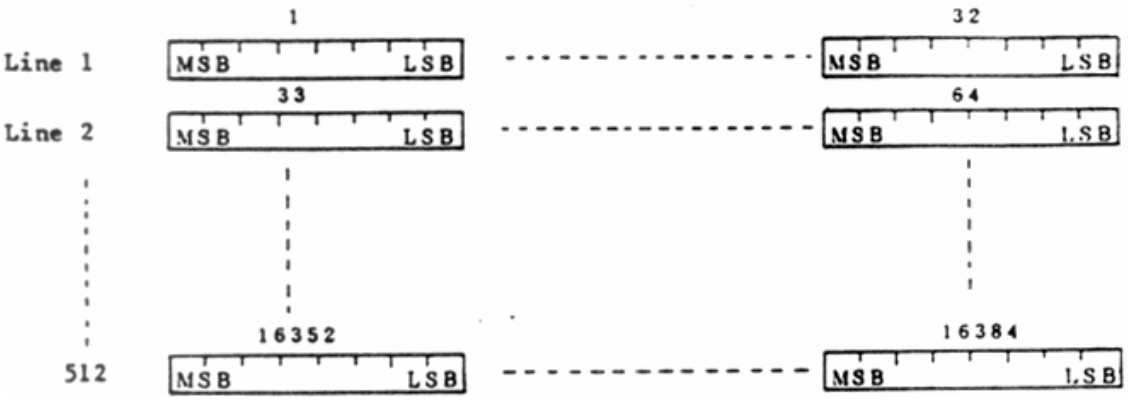
- Both n1 and n2 are two-digit hexadecimal numbers. Here n1 specifies the lower two digits while n2 specifies the upper two digits in hexadecimal notation.

o Set n1 and n2 as follows when specifying the maximum number of print lines (65536 dot lines)

n1 ⇨ 00H
n2 ⇨ 00H

[Graphic mode input example] (512-dot line print)





To print the above 512 dot lines, it is necessary to transfer ?32 bytes) x (512 dot lines) = 16384 bytes?of graphic data.

Notes:
1. If, in graphic mode, data transmission speed is decreased or data transmission is interrupted in the middle of transmission, the motor is automatically stopped and printer will not restart operation until the following data is entered.
2. After graphic printing has terminated, 3-dot line space is set between the print terminating position and the subsequent character or graphic print starting position.

Fig. 2 Data transmission sequence

Fig. 3 Timing chart

Fig. 4 Printer and controller exterior appearances

Table 1

Table 2

Code	Function
NUL	No operation
CR	Releases double-width enlarged character print mode
LF	Prints out buffer data and executes carriage return
FF	Prints out buffer data and feeds pages
SO	Sets double-width enlarged character print mode
SI	Releases double-width enlarged character print mode
RS	Black-and-white reversed printing (valid only in graphic mode)
US	Releases black-and-white-reversed-print mode
ESCCn	Page length selection command
ESCVn1, n2	Graphic mode selection command
ESC R	Reversed character print mode selection command
ESC S	Releases reversed character print mode

4 OTHERS

4.1 Character Print Example

The character print example is shown on page 28.

4.2 Notes on Use

(1) No foreign matters shall be attached or entered around the print head.

(2) When installing the printer, use the rubber washer attached. Stick the washer to the screw section on the bottom and install the printer. (The recommended clamping torque of the screw is 4 to 5 Kg-cm.)

(3) When handling the controller, take note for shortcircuit, etc.

(4) If connectors are inserted or removed while the power is being turned ON, the elements may be damaged.
Therefore, connectors must be inserted or removed after the power has been turned OFF.

4.3 Options

(1) Power supply (FTP-040Z-01/02)

- o Input voltage 100 VAC ± 12% 50/60 Hz
- o Output voltage

FTP-040Z-01 — 5V - 1A, 24V - 2.5A

FTP-040Z-02 — 5V - 2.5A, 24V - 2.5A